



# **Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform**

## **Design Guide**

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*March 2002*

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## Revision History

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Revision	Description	Date
-001	Initial Release.	February 2002
-002	Changed: Section 6.3; DDR Command Clock Figure Notes Added: Section 12.5.4; New P64H2 Power Sequencing Requirement Updated Schematics to reflect changes identified above.	March 2002

# Introduction

# 1

The *Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform Design Guide* documents Intel's design recommendations for systems based on the Intel® Xeon™ Processor with 512 KB L2 Cache and the E7500 chipset. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document addresses system design issues such as power delivery.

Carefully follow the design information, board schematics, debug recommendations, and system checklists provided in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

Note that the guidelines recommended in this document are based on experience and simulation work done at Intel while developing Intel Xeon processor with 512 KB L2 cache / E7500 chipset-based systems. This work is ongoing, and the recommendations are subject to change.

Board designers may use the associated Intel schematics as a reference. While the schematics cover a specific design implementation, the core schematics remain the same for most E7500 chipset-based platforms. The schematic set provides a reference schematic for each E7500 chipset component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

## 1.1 Reference Documentation

**Note:** For the latest revision and documentation number, contact your appropriate field representative.

**Table 1-1. Reference Documents**

Document	Document Number/Source
603-Pin Socket Design Guidelines	<a href="http://developer.intel.com/design/Xeon/guides/249672.htm">http://developer.intel.com/design/Xeon/guides/249672.htm</a>
82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Datasheet	
APIC External Design Specification	
AT Attachment - 6 with packet Interface (ATA/ATAPI - 6)	
CK-408B Clock Synthesizer/Driver Specification Revision 1.1	
ITP700 Debug Port Design Guide	<a href="http://developer.intel.com/design/Xeon/guides/">http://developer.intel.com/design/Xeon/guides/</a>
Intel® Xeon™ Processor with 512 KB L2 Cache Signal Integrity Models	<a href="http://developer.intel.com/design/Xeon/devtools">http://developer.intel.com/design/Xeon/devtools</a>
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet	290733
Intel® PCI-64 Hub 2 (P64H2) Thermal and Mechanical Design Guidelines	298648
Intel® E7500 Chipset Thermal and Mechanical Design Guidelines	298647
Intel® PCI-64 Hub 2 (P64H2) Datasheet	290732
Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet	290730

Table 1-1. Reference Documents

Document	Document Number/Source
<i>PCI Bus Power Management Interface Specification, Revision 1.1</i>	<a href="http://www.pcisig.com/specifications/pci_bus_power_management_interface">http://www.pcisig.com/specifications/pci_bus_power_management_interface</a>
<i>PCI Hot Plug Specification, Revision 1.1</i>	<a href="http://www.pcisig.com/specifications/pci_hot_plug">http://www.pcisig.com/specifications/pci_hot_plug</a>
<i>PCI Local Bus Specification, Revision 2.2</i>	<a href="http://www.pcisig.com/specifications/conventional_pci">http://www.pcisig.com/specifications/conventional_pci</a>
<i>PCI-PCI Bridge Architecture Specification, Revision 1.1</i>	<a href="http://www.pcisig.com/specifications/pci_to_pci_bridge_architecture">http://www.pcisig.com/specifications/pci_to_pci_bridge_architecture</a>
<i>PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0</i>	<a href="http://www.pcisig.com/specifications/pci_hot_plug">http://www.pcisig.com/specifications/pci_hot_plug</a>
<i>PCI-X Specification, Revision 1.0a</i>	<a href="http://www.pcisig.com/specifications/pci_x">http://www.pcisig.com/specifications/pci_x</a>
<i>System Management Bus Specification (SMBus), Revision 1.1</i>	<a href="http://www.smbus.org/specs/">http://www.smbus.org/specs/</a>
<i>Universal Serial Bus Specification, Revision 1.1</i>	<a href="http://www.usb.org/developers/docs.html">http://www.usb.org/developers/docs.html</a>
<i>VRM 9.1 DC-DC Converter Design Guidelines</i>	<a href="http://developer.intel.com/design/Xeon/guides/">http://developer.intel.com/design/Xeon/guides/</a>
<i>Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines</i>	<a href="http://developer.intel.com/design/Xeon/guides/">http://developer.intel.com/design/Xeon/guides/</a>
<i>Intel® Xeon™ Processor with 512 KB L2 Cache System Compatibility Guidelines</i>	<a href="http://developer.intel.com/design/Xeon/guides/">http://developer.intel.com/design/Xeon/guides/</a>
<i>Intel® Xeon™ Processor Thermal Design Guidelines</i>	<a href="http://developer.intel.com/design/Xeon/guides/298348.htm">http://developer.intel.com/design/Xeon/guides/298348.htm</a>
<i>Intel® Xeon™ Processor Thermal Solution Functional Specifications</i>	<a href="http://developer.intel.com/design/Xeon/applnots/249673.htm">http://developer.intel.com/design/Xeon/applnots/249673.htm</a>
<i>Intel® Xeon™ Processor with 512 KB L2 Cache Thermal Models</i>	<a href="http://developer.intel.com/design/Xeon/devtools/">http://developer.intel.com/design/Xeon/devtools/</a>
<i>Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Model in IGES Format</i>	<a href="http://developer.intel.com/design/Xeon/devtools/">http://developer.intel.com/design/Xeon/devtools/</a>
<i>Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Model in ProE* Format</i>	<a href="http://developer.intel.com/design/Xeon/devtools/">http://developer.intel.com/design/Xeon/devtools/</a>
<i>Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet</i>	<a href="http://developer.intel.com/design/Xeon/datashts/298642.htm">http://developer.intel.com/design/Xeon/datashts/298642.htm</a>
<i>AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions</i>	<a href="http://developer.intel.com/design/chipsets/applnots/292276.htm">http://developer.intel.com/design/chipsets/applnots/292276.htm</a>



## 1.2 Conventions and Terminology

This section defines conventions and terminology used throughout the design guide.

Convention/Terminology	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The Xeon™ processor family system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	Xeon processors do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWROOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as "Asynchronous GTL+ Signals". However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Core Power	Core power refers to a power rail that is on only during full-power operation. These power rails are on when the active-low PSON signal is asserted to the power supply. The core power rails that are distributed directly from the power supply are: +12 V, +5 V, and +3.3 V.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. <ul style="list-style-type: none"> <li>Backward Crosstalk – Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.</li> <li>Forward Crosstalk – Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal.</li> <li>Even Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching.</li> <li>Odd Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.</li> </ul>
Derived power	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, +2.5 V is derived from a +5 V power rail using a voltage regulator.
Dual Processor (DP)	Used to specify a system configuration using two processors.
Electromagnetic Compatibility (EMC)	The successful operation of electronic equipment in its intended electromagnetic environment.
Electromagnetic Interference (EMI)	Electromagnetic radiation from an electrical source that interrupts the normal function of an electronic device.

Convention/Terminology	Description
Flight Time	<p>Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the <math>T_{co}</math> of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as:</p> <ul style="list-style-type: none"> <li>The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings.</li> <li>Maximum and Minimum Flight Time – Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects.</li> <li>Maximum flight time is the largest acceptable flight time that a network experiences under all conditions.</li> <li>Minimum flight time is the smallest acceptable flight time that a network experiences under all conditions.</li> </ul>
Full-power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant) state.
GTLREF	Reference voltage for AGTL+ input pins.
Inter-Symbol Interference (ISI)	The effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line, and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	"Power-Good," "PWRGOOD," or "CPUPWRGOOD" (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Power Rails	A power supply has five power rails: +12 V, -12 V, +5 V, +3.3 V, and +5 VSB. In addition to these power rails from the power supply, several other power rails are created by voltage regulators on the Reference Board.
Ringback	The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the bus which connects the processor to the platform.
Setup Window	The time between the beginning of Setup to Clock ( $TSU\_MIN$ ) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Convention/Terminology	Description
Simultaneous Switching Output (SSO)	Effects which are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay ("push-out") or a decrease in propagation delay ("pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Standby Power Rail	Standby power is supplied by the power supply during times when the system is powered down. The purpose is to maintain functions that always need to be enabled, such as the date and time-of-day within the BIOS. The power supply provides a +5 VSB power rail.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
VCC_CPU	VCC_CPU is the core power for the processor. The system bus is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VRM 9.1	"VRM 9.1" refers to the Voltage Regulator Module specification for the Xeon processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

## 1.3 System Overview

The E7500 chipset is Intel's first generation server chipset designed for use with the Xeon processor. The architecture of the chipset provides the performance and feature-set required for dual-processor based servers in the entry-level and mid-range, front-end and general-purpose server market segments. A new chipset component interconnect, the Hub Interface 2.0 (HI2.0), is designed into the E7500 chipset to provide more efficient communication between chipset components for high-speed I/O. Each HI2.0 provides 1.066 GB/s I/O bandwidth. The E7500 MCH has three HI2.0 connections, delivering 3.2 GB/s bandwidth for high-speed I/O, which can be used for PCI/PCI-X bridges. The system bus, used to connect the processor with the E7500 chipset, utilizes a 400 MHz transfer rate for data transfers, delivering 3.2 GB/s. The E7500 chipset architecture supports a 144-bit wide, 200 MHz DDR memory interface also capable of transferring data at 3.2 GB/s.

In addition to these performance features, E7500 chipset-based platforms also provide the RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features required for entry-level and mid-range servers. These features include: Chipkill\* technology ECC for memory, ECC for all high-performance I/O, out-of-band manageability through SMBus target interfaces on all major components, memory scrubbing and auto-initialization, processor thermal monitoring, and hot-plug PCI. For a complete list of the features on this platform, refer to the component datasheets listed in [Section 1.1](#).

### 1.3.1 Intel® Xeon™ Processor with 512 KB L2 Cache

The Intel Xeon processor with 512 KB L2 cache is the second generation of microprocessors targeted for servers and workstations using the Intel® NetBurst™ microarchitecture. The Xeon processor delivers performance levels that are significantly higher than previous generations of IA-32 processors. The E7500 chipset supports all speeds of the Intel Xeon processor with 512 KB L2 cache.

**Table 1-2. Intel® Xeon™ Processor with 512 KB L2 Cache Feature Set Overview**

Feature	Xeon™
L2 Cache	512 KB
Data Bus Transfer Rate	3.2 GB/s
Multi-Processor Support	1–2 CPUs
Manageability Features	Intel and OEM EEPROMs and thermal sensor on package
Package	603-pin micro-PGA
Operating Voltage	1.50 V

Unless otherwise noted, the term “processor” refers to the Xeon processor.

The Xeon processor includes the following advanced microarchitecture features:

- Hyper Pipelined Technology.
- Advanced Dynamic Execution.
- Execution Trace Cache.
- Streaming SIMD (single instruction, multiple data) Extensions 2.
- Advanced Transfer Cache.
- Enhanced Floating Point and Multimedia Engine.

The Intel Xeon processor system bus utilizes a split-transaction, deferred reply protocol similar to that of the Intel® Pentium® III Xeon™ processor bus, however the system bus is not compatible with the Pentium III Xeon processor bus. The system bus uses source-synchronous transfer of address and data to improve performance and enables addressing at 2X the system bus frequency of 100 MHz and data transfers at 4X the system bus frequency of 100 MHz. This allows the processors to transfer data at 3.2 GB/s.

The Xeon processor provides manageability features consistent with Intel® Pentium® III Xeon™ processors. These features include the Processor Information ROM, the OEM EEPROM, and the processor thermal sensor; all of which are accessed through the System Management Bus (SMBus). The Processor Information ROM is a 128-byte read-only device that incorporates Intel processor specific data. The OEM EEPROM, also known as the “scratchpad EEPROM,” is a 128-byte read/write EEPROM in which an OEM may program system specific data. The thermal sensor monitors the temperature of the processor die.

## 1.3.2 Intel® E7500 Chipset

The E7500 chipset consists of three major components: the Intel® E7500 Memory Controller Hub (referred to throughout this document as the MCH), the Intel® 82801CA I/O Controller Hub 3-S (hereafter referred to as ICH3-S), and the Intel® 82870P2 PCI/ PCI-X 64-bit Hub 2 (abbreviated to P64H2). The chipset components communicate via hub interfaces (HIs). The MCH provides four hub interface connections: one for the ICH3-S and three for high-speed I/O using 82870P2 P64H2 components. The hub interfaces are point-to-point and therefore only support two agents (the MCH plus one I/O device). Therefore, the system supports a total of three P64H2s.

### 1.3.2.1 Intel® E7500 Memory Controller Hub (MCH)

The MCH is a 1005-ball FC-BGA package and contains the following functionality:

- System Bus Features:
  - Supports dual processors at 100 MHz (x4 transfers).
  - System bus bandwidth of 3.2 GB/s (400 MHz).
  - Supports 36-bit system bus addressing model.
  - 12 deep in-order queue, 2 deep defer queue.
- Memory Bus Features:
  - 144-bit wide, DDR-200 memory interface with memory bandwidth of 3.2 GB/s.
  - Supports x72, ECC, registered DDR-200 DIMMs using 64-Mb, 128-Mb, 256-Mb and 512-Mb DRAMs.
  - Supports a maximum of 16 GB of memory.
  - Supports Single 4-bit Error Correct, Double 4-bit Error Detect (S4EC/D4ED) Chipkill technology ECC (x4 Chipkill technology).
  - Supports up to 32 simultaneous open pages.
- I/O Features:
  - Provides HI1.5 connection for ICH3-S (Hub Interface A):
    - 266 MB/s point-to-point connection for ICH3-S with parity protection.
    - 8-bit wide, 66 MHz base clock, 4X data transfer.
    - Parallel termination mode for longer trace lengths.
    - 64-bit inbound addressing, 32-bit outbound addressing.
  - Provides 3 HI2.0 Connections for P64H2s (Hub Interfaces B, C and D):
    - 1.066 GB/s point-to-point connection for I/O bridges with ECC protection.
    - 16-bit wide, 66 MHz base clock, 8X data transfer.
    - Parallel termination mode for longer trace lengths.
    - 64-bit inbound addressing, 32-bit outbound addressing.
- Power Management Features:
  - Supports C0, C1, C2, S0, S1, S4, and S5 power states. **(Does not support C3, C4, S2, and S3).**

### 1.3.2.2 I/O Controller Hub 3 (Intel® ICH3-S)

The I/O Controller Hub (ICH3-S) provides the legacy I/O subsystem for E7500 chipset-based platforms. Additionally, it integrates many advanced I/O functions. The ICH3-S includes the following features:

- Provides HI1.5 Connection to MCH:
  - 266 MB/s point-to-point connection for ICH3-S with parity protection.
  - 8-bit wide, 66 MHz base clock, 4X data transfer.
  - Parallel termination mode for longer trace lengths.
  - 64-bit inbound addressing, 32-bit outbound addressing.
- 2 channel Ultra ATA/100 bus master IDE controller.
- 3 Universal Host Controller Interface (UHCI) USB 1.1 compliant host controllers (Capabilities for six ports).
- I/O APIC.
- *System Management Bus (SMBus) Specification, Version 1.1* compliant controller.
- LPC interface.
- *AC '97 Component Specification, Revision 2.2* compliant interface.
- *PCI Local Bus Specification, Revision 2.2* compliant interface.
- Integrated LAN Controller.

### 1.3.2.3 PCI/PCI-X 64-bit Hub 2 (Intel® 82870P2 P64H2)

The P64H2 provides PCI/PCI-X, high-performance I/O capability on E7500 chipset based platforms. Each P64H2 component includes:

- 16-bit, HI2.0 Connection to MCH:
  - 1 GB/s point-to-point connection for I/O bridges with ECC protection.
  - 16-bit wide, 66 MHz base clock, 8X data transfer.
  - Parallel termination mode for longer trace lengths.
  - 64-bit inbound addressing, 32-bit outbound addressing.
- Two Independent, 64-bit PCI/PCI-X Interfaces:
  - *PCI-X Specification, Revision 1.0a* compliant.
  - *PCI Local Bus Specification, Revision 2.2* compliant.
  - *PCI-PCI Bridge Architecture Specification, Revision 1.1* compliant.
  - *PCI Hot Plug Specification, Revision 1.1* compliant.
  - One PCI Hot Plug Controller (PHPC) per PCI/PCI-X interface.
  - One IOxAPIC per PCI/PCI-X Interface (16 external, 8 internal interrupts).
  - SMBus target for access to all internal PCI registers.

### 1.3.3 Bandwidth Summary

Table 1-3 describes the clock maximum speed, sample rate, and bandwidth for each of the interfaces in the E7500 chipset based platform.

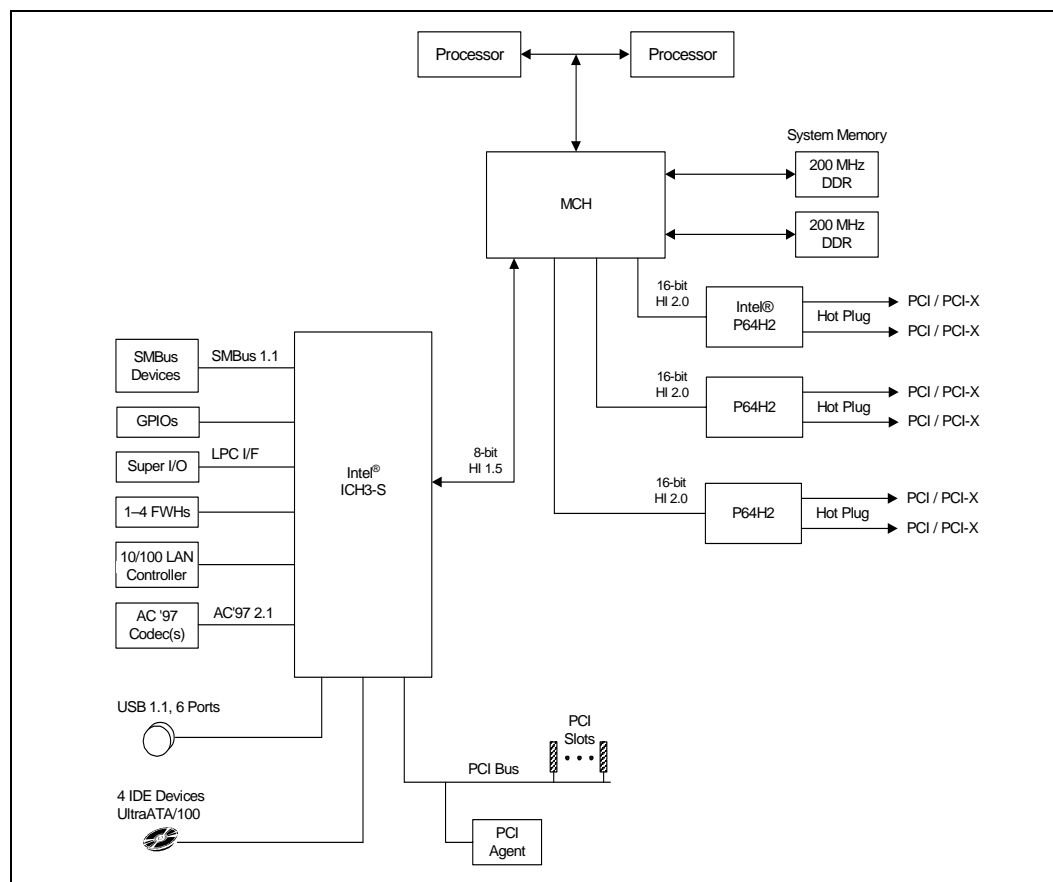
**Table 1-3. Platform Maximum Bandwidth Summary**

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus (Data)	100	4	8	3200
DDR Interface	100	2	16	3200
Hub Interface A	66	4	1	266
Hub Interface B, C, D	66	8	2	1066
PCI-X	133	1	8	1066

### 1.3.4 System Configurations

Figure 1-1 illustrates an example E7500 chipset-based system configuration for server platforms using Xeon processors.

**Figure 1-1. Example Intel® Xeon™ Processor with 512 KB L2 Cache / Intel® E7500 Chipset Based System Configuration**



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# Component Quadrant Layout

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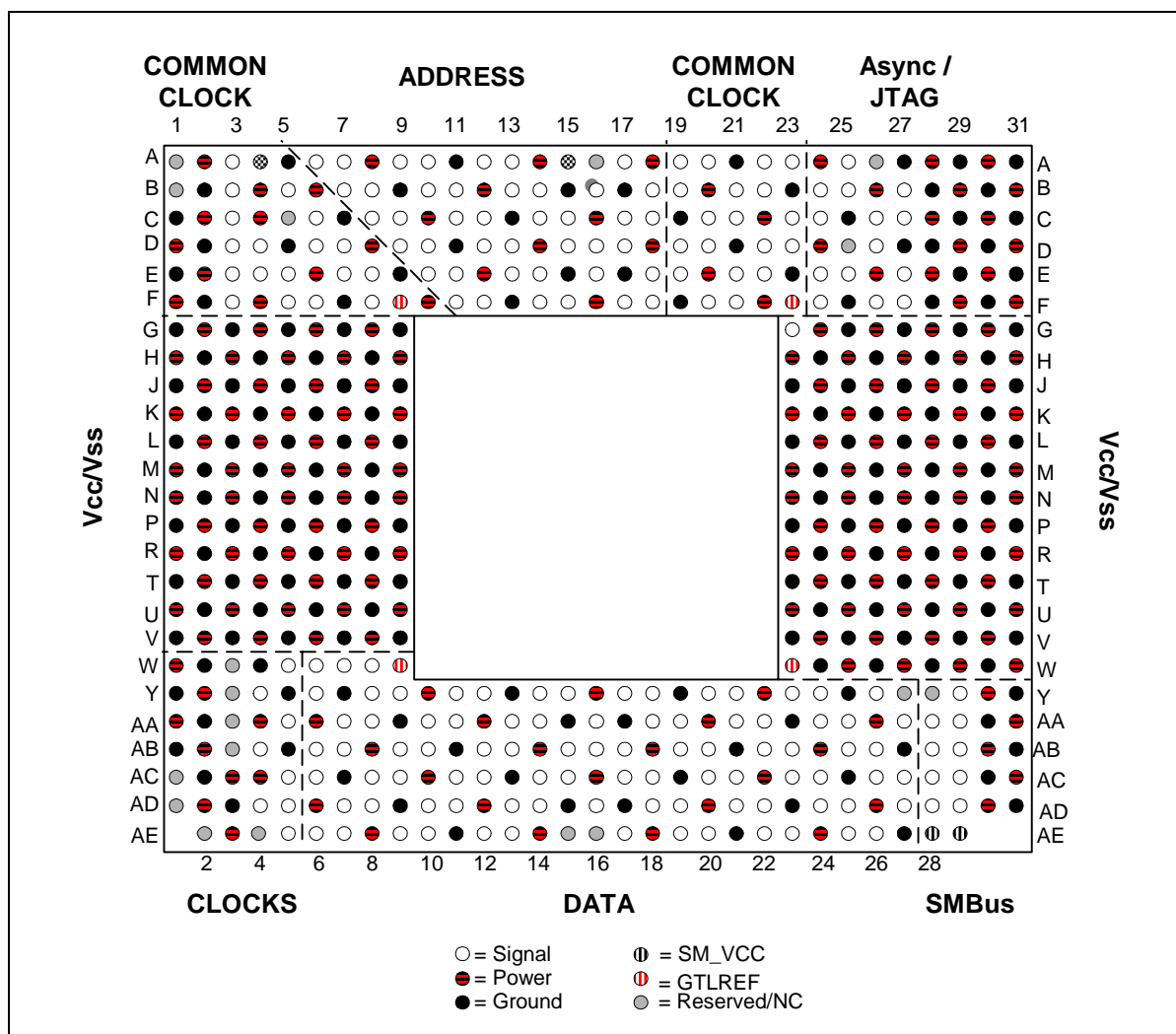
## 2

The following figures show only general quadrant information, not exact component ball count. Designers should use only the exact ball assignment to conduct routing analyses. Reference the following documents for exact ball assignment information.

- *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet*
- *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*
- *Intel® PCI-64 Hub 2 (P64H2) Datasheet*
- *Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet*

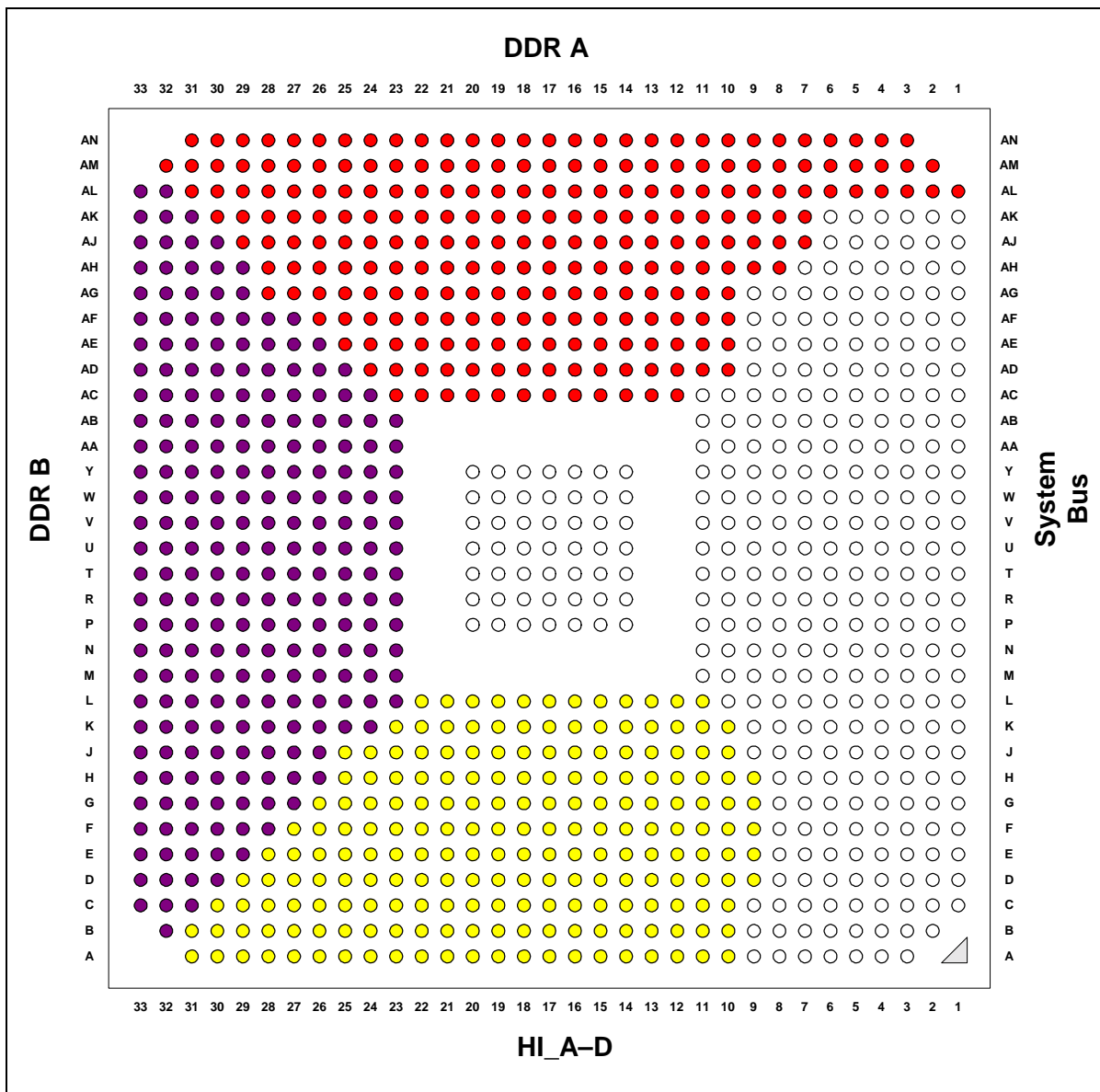
## 2.1 Intel® Xeon™ Processor with 512 KB L2 Cache Quadrant Layout

Figure 2-1. Intel® Xeon™ Processor with 512 KB L2 Cache Quadrant Layout (Top View)



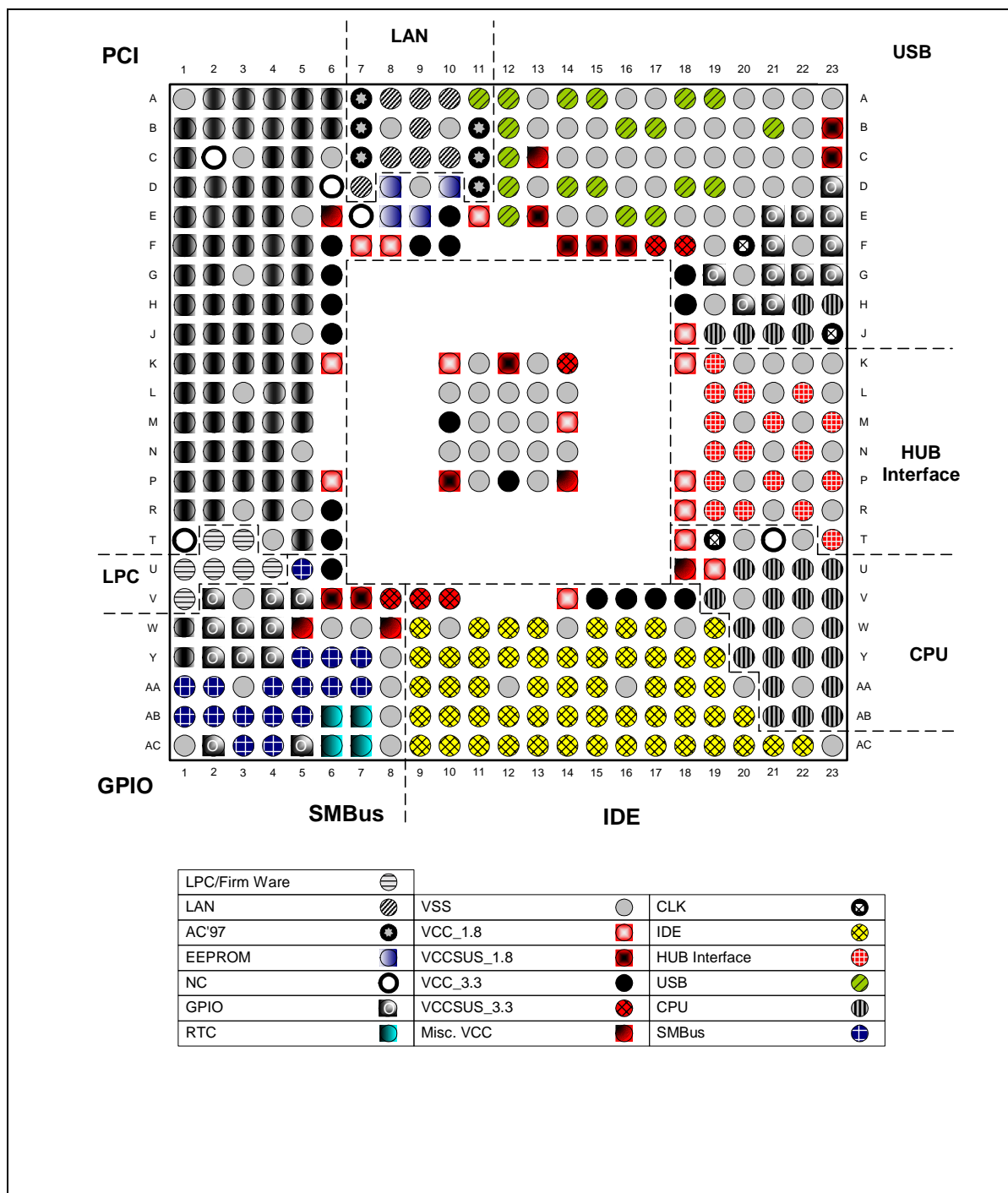
## 2.2 Intel® E7500 MCH Quadrant Layout

Figure 2-2. Intel® E7500 MCH Quadrant Layout (Top View)



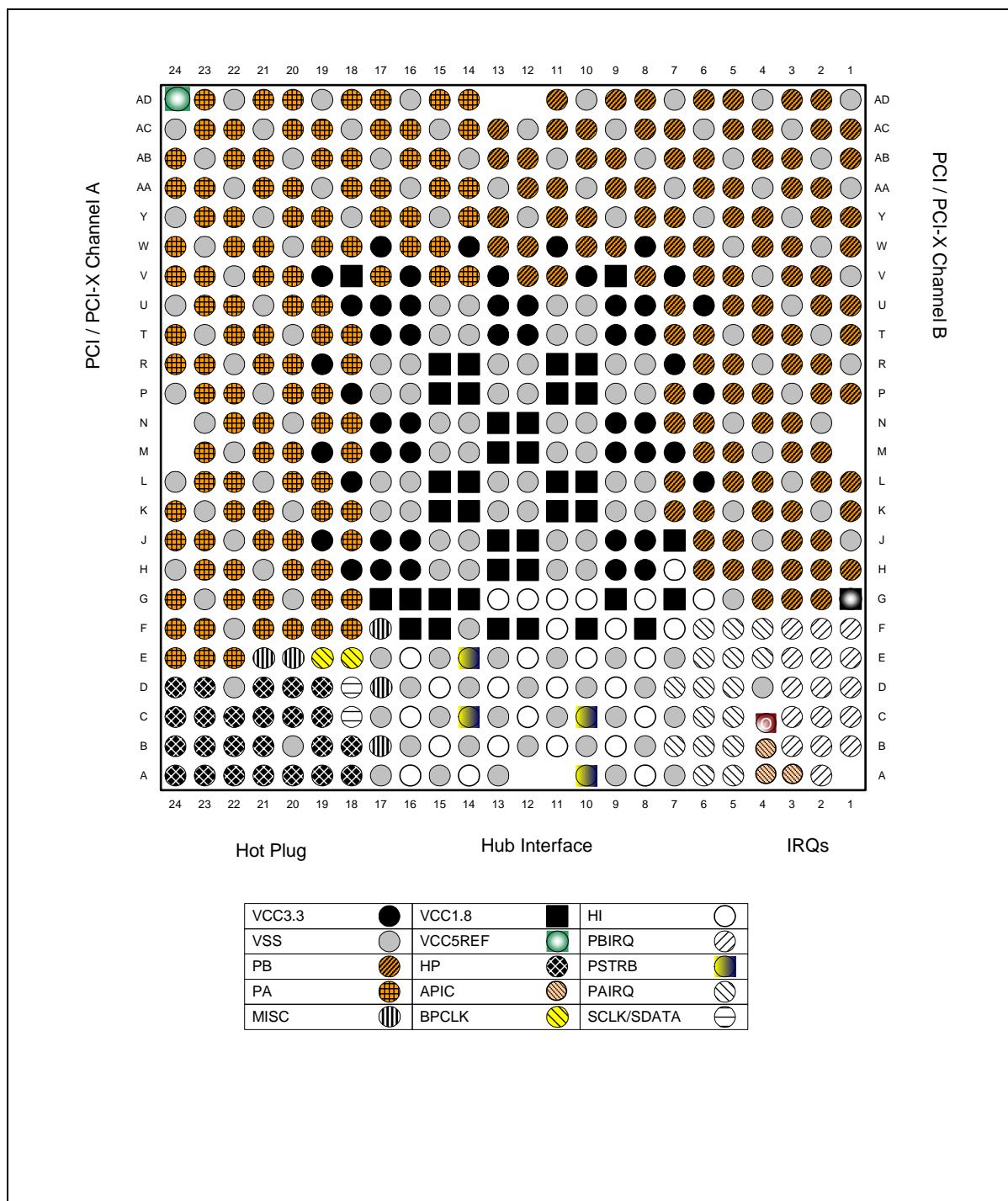
## 2.3 Intel® ICH3-S Quadrant Layout

Figure 2-3. Intel® ICH3-S Quadrant Layout (Top View)



## 2.4 Intel® 82870P2 P64H2 Quadrant Layout

Figure 2-4. Intel® P64H2 Quadrant Layout (Top View)



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# Platform Stack-Up and Component Placement Overview

## 3

### 3.1 Platform Component Placement

Figure 3-1 illustrates the component placement for the Intel Xeon processor with 512 KB L2 cache/Intel E7500 chipset-based customer reference board (E7500 CRB). Table 3-1 lists the assumptions used for the component placement. Refer to [www.ssiforum.org](http://www.ssiforum.org) for detailed information on the SSI (Server System Infrastructure) specification.

**Table 3-1. Assumptions for System Placement Example**

System Configuration	Assumptions		
	Form Factor (SSI Specification)	Number of PCB Layers	Assembly
DP Server	Midrange Electronic-Bay (13"x16")	8 Layers	Double Sided

## 3.2 Platform Stack-Up

Figure 3-1. Intel® E7500 Chipset Customer Reference Board System Placement Example

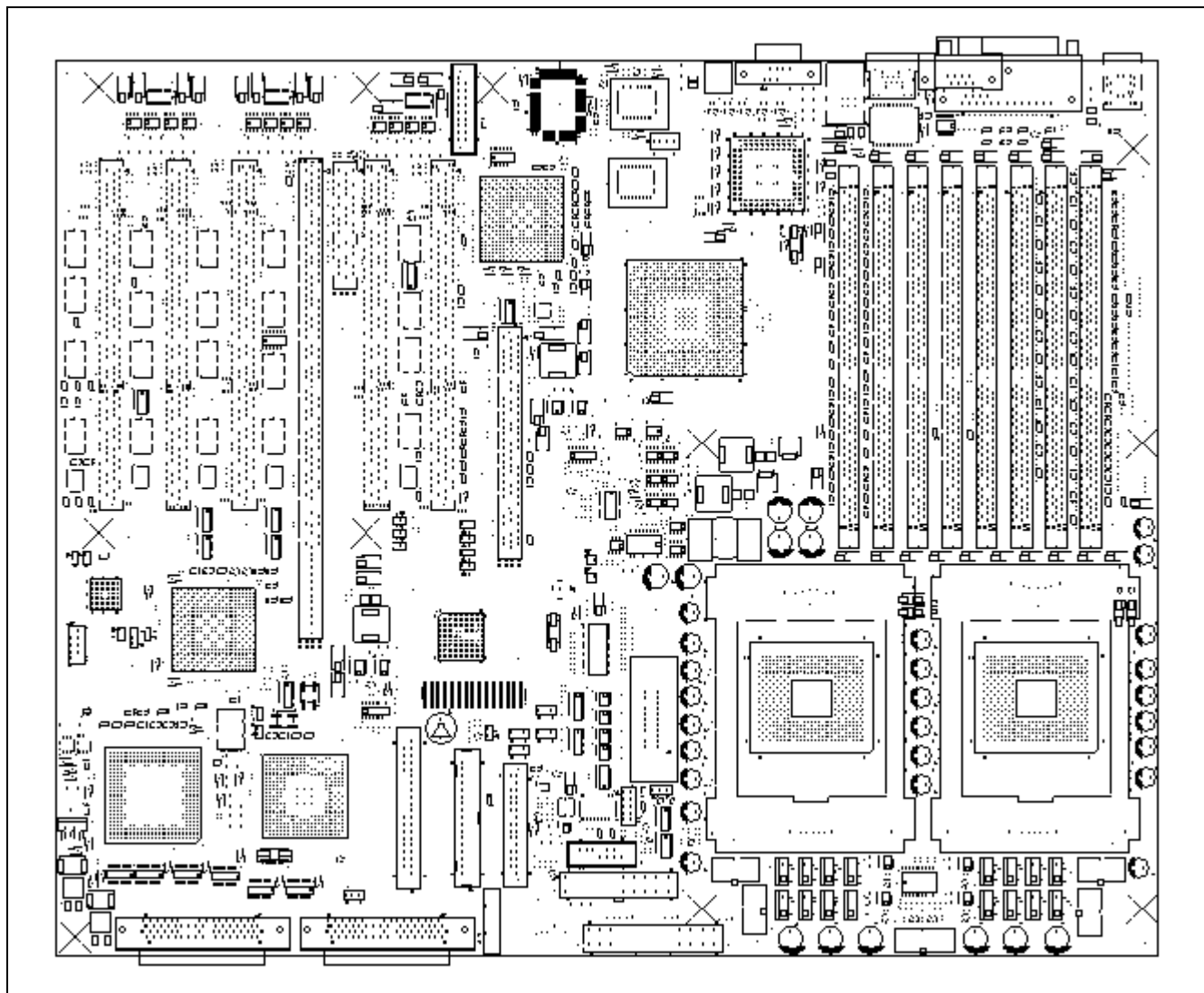
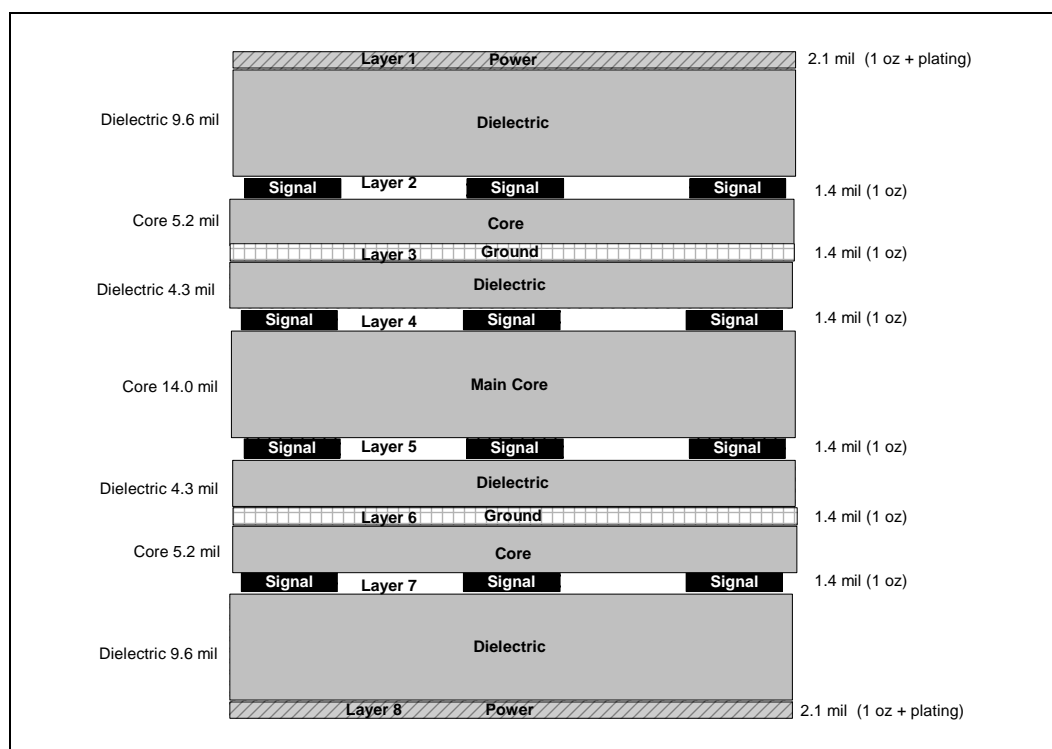


Figure 3-2 shows the recommended platform stack-up. All layers are 1 oz copper. The processor requires 2 oz of copper to deliver power and 2 oz of copper to deliver ground. Vias are 10 mil finished hole with 35 mil anti-pads and 24 mil pads.

Route signal layers as asymmetric stripline on layers 2, 4, 5 and 7. The signal layers must reference ground on layer 3 or layer 6 only. Route signals on layers 4 and 5 orthogonally to reduce crosstalk between the layers.

Intel strongly recommends that system designers use the stack-up shown in Figure 3-2 and recommendations in Table 3-2 when designing their boards. Intel realizes numerous ways exist to achieve these targeted impedance tolerances; contact your board vendor for these specifics. Intel encourages platform designers to perform comprehensive simulation analysis to ensure all timing specifications are met. This is particularly important if a design deviates from the design guidelines provided.



**Figure 3-2. 8 Layer, 50  $\Omega$  Board with 5 mil Traces**

**Table 3-2. E7500 Chipset Customer Reference Board Requirements**

Board Factor	Recommendation
Material	<ul style="list-style-type: none"> <li>Standard FR4 Tg 170 Epoxy.</li> </ul>
Impedance Requirements	<ul style="list-style-type: none"> <li>50 <math>\Omega</math> impedance <math>\pm 10\%</math> Layers 2,4,5,7 (except lower left corner SCSI interface).</li> <li>SCSI interface 83 <math>\Omega</math> single ended, 122 <math>\Omega</math> differential pair <math>\pm 10\%</math> (layers 1 and 8 lower left corner).</li> </ul>
Etch	<ul style="list-style-type: none"> <li>5 mil trace width and space minimum inner/outer.</li> <li>SCSI interface; 6 mil separation within a pair, 20 mil space between adjacent pairs.</li> </ul>
Finished Via Size	<ul style="list-style-type: none"> <li>Minimum via size is 0.014 mil finished in a 0.026 mil land with 0.040 mil antipad.</li> <li>Approximately 15,000 plated through holes total.</li> </ul>
Finish	<ul style="list-style-type: none"> <li>Solder Mask On Bare Copper (SMOBC)</li> </ul>
Soldermask Type	<ul style="list-style-type: none"> <li>SM-840 minimum web 0.004 mils.</li> </ul>
Fabrication	<ul style="list-style-type: none"> <li>Edge Routed.</li> </ul>
Component Technology	<ul style="list-style-type: none"> <li>Through hole / SMT.</li> <li>QFP, BGA, Front side.</li> <li>Discrete 0603, 0805 Back side.</li> </ul>

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# Platform Clock Routing Guidelines 4

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To minimize jitter, improve routing, and reduce cost, E7500 chipset-based systems should use a single chip clock solution, the CK408B. In this configuration, the CK408B provides four, 100 MHz differential outputs pairs for all of the bus agents, including the ITP connector, and five, 66 MHz speed clocks that drive all I/O buses. [Figure 4-1](#) shows the implementation of the bus clocks for this configuration.

For more information on CK408B compliance, refer to the *CK408B Clock Synthesizer Specification Specifically for E7500 Chipset DP with ITP System Clock Generator* Document.

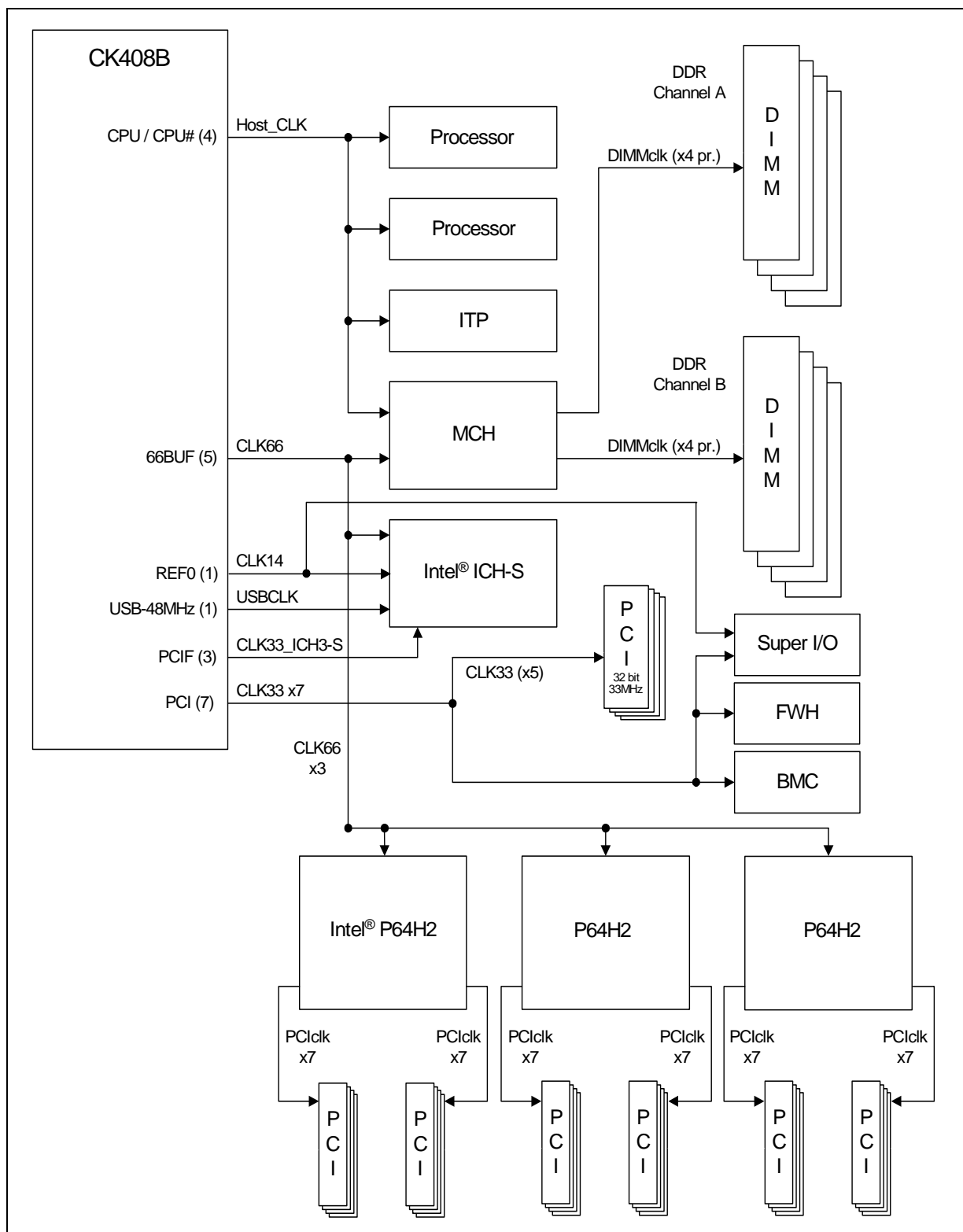
**Table 4-1. CK408B Clock Groups**

Clock Group Name	Frequency (MHz)	Receiver
Host_CLK	100	Processor 0, Processor 1, Debug Port and MCH
CLK66	66	MCH, ICH3-S, and P64H2
CLK33_ICH3-S	33	ICH3-S
CLK14	14.318	ICH3-S and SIO
CLK33	33	PCI Connector, SIO, BMC, and FWH
USBCLK	48	ICH3-S

Table 4-2. Platform System Clock-Reference

Clock Group	CK-408B Pin	Component	Component Pin Name
Host_CLK	CPU#	Debug Port	BCLK[0]
	CPU	Debug Port	BCLK[1]
	CPU#	Processor 0	BCLK[0]
	CPU	Processor 0	BCLK[1]
	CPU#	Processor 1	BCLK[0]
	CPU	Processor 1	BCLK[1]
	CPU#	MCH	HCLKINP
	CPU	MCH	HCLKINN
CLK66	66BUF	MCH	66IN
		ICH3-S	CLK66
		P64H2	CLK66
CLK33_ICH3-S	PCIF	ICH3-S	PCICLK
CLK14	REF0	ICH3-S	CLK14
		SIO	CLOCKI
CLK33	PCI	PCI Connector #1	CLK
		PCI Connector #2	CLK
		PCI Connector #3	CLK
		PCI Connector #4	CLK
		PCI Connector #5	CLK
		FWH	CLK
		SIO	PCI_CLK
	PCIF	BMC	LCLK
USBCLK	USB-48MHZ	ICH3-S	CLK48

**Figure 4-1. Intel® E7500 Chipset-Based System Clocking Diagram**



## 4.1 Clock Groups

### 4.1.1 HOST\_CLK Clock Group

#### 4.1.1.1 HOST\_CLK Clock Topology

The clock synthesizer provides four sets of 100 MHz differential clock outputs. The 100 MHz differential clocks are driven to the Processors, the MCH, and the processors' debug port as shown in Figure 4-1.

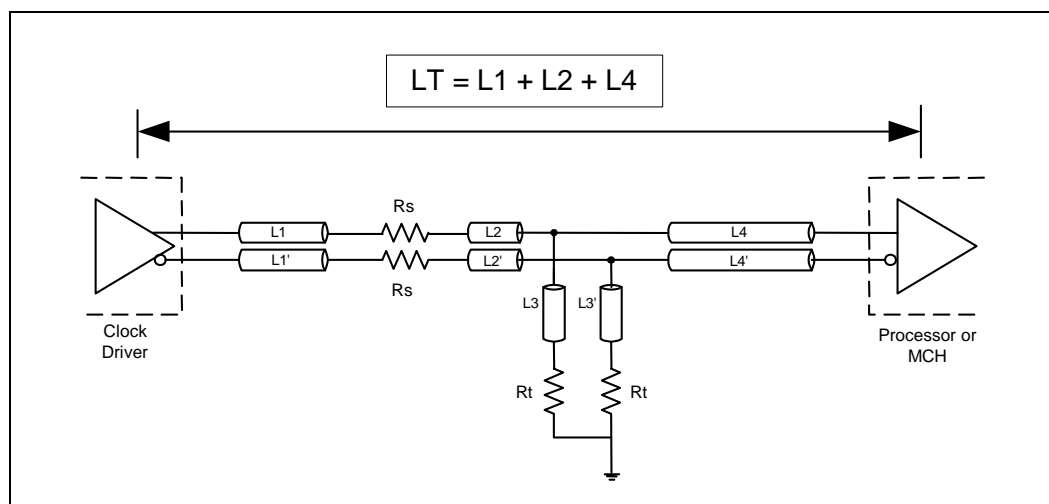
The clock driver differential bus output structure is a “Current Mode Current Steering” output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors “ $R_t$ .” The resulting amplitude is determined by multiplying  $I_{OUT}$  by the value of  $R_t$ . The current  $I_{OUT}$  is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of “ $R$ ” to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a “Shunt Source Termination.” Refer to Figure 4-2 for an illustration of this termination scheme. Parallel  $R_t$  resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors “ $R_s$ ” provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor  $R_t$ .

The value of  $R_t$  should be selected to match the characteristic impedance of the motherboard, and  $R_s$  should be between  $20\ \Omega$  and  $33\ \Omega$ . Simulations have shown that  $R_s$  values above  $33\ \Omega$  provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin #43) is pulled high – making the multiplication factor 6.
- Iref pin (pin # 42) is connected to ground through a  $475\ \Omega \pm 1\%$  resistor – making the  $I_{ref}$  2.32 mA.

Figure 4-2. Source Shunt Termination



**Table 4-3. HOST\_CLK[1:0]# Routing Guidelines**

Layout Guideline	Value	Illustration	Notes
HOST_CLK Skew between Agents	300 ps total budget: 150 ps for clock driver 150 ps for interconnect	Figure 4-2 and Figure 4-3	1,2,3,4
Trace Width	5 mils	Figure 4-4	
Differential Pair Spacing	20 – 25 mils	Figure 4-4	5,6
Spacing to Other Traces	25 mils	Figure 4-4	
Serpentine Spacing	Maintain a minimum S/h ratio of > 5/26 Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends, if possible.	Figure 4-4	
Motherboard Impedance – Differential	100 $\Omega$ typical		8
Motherboard Impedance – Single Ended	50 $\Omega \pm 10\%$		9
Processor Routing Length – L1, L1': Clock Driver to Rs	0 – 0.5"	Figure 4-2	13
Processor Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2"	Figure 4-2	13
Processor Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2"	Figure 4-2	13
Processor Routing Length – L4, L4': Rs-Rt Node to Load	0 – 22"	Figure 4-2	
MCH Routing Length – L1, L1': Clock Driver to Rs	0 – 0.5"	Figure 4-2	13
MCH Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2"	Figure 4-2	13
MCH Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2"	Figure 4-2	13
MCH Routing Length – L4, L4': Rs-Rt Node to Load	0 – 22"	Figure 4-2	
Processor to MCH Length Matching (LT)	0.035" $\pm$ 0.010" MCH LT must be 0.076" longer than Processor LT.	Figure 4-2	10
Processor to Processor Length Matching (LT)	$\pm 10$ mils	Figure 4-2	15
HOST_CLK0 – HOST_CLK1 Length Matching	$\pm 10$ mils		
Rs Series Termination Value	20 – 33 $\Omega \pm 5\%$	Figure 4-2	11
Rt Shunt Termination Value	49.9 $\Omega \pm 1\%$ (for 50 $\Omega$ board impedance)	Figure 4-2	12

**NOTES:**

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.

4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this degrades the noise rejection of the network.
7. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
8. The differential impedance of each clock pair is approximately  $2 \cdot Z_{\text{single-ended}} \cdot (1 - 2 \cdot K_b)$  where  $K_b$  is the backwards cross-talk coefficient. For the recommended trace spacing,  $K_b$  is very small, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the HOST\_CLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the motherboard trace length for the chipset will be longer than that for the processor.
11.  $R_s$  values between  $20 \Omega$  and  $33 \Omega$  have been shown to be effective.
12.  $R_t$  shunt termination value should match the motherboard impedance.
13. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
14. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in  $E_r$  and the impedance variations due to physical tolerances of circuit board material.
15. Length of LT for one processor must match the LT of all other HOST\_CLK traces to other processor with specified tolerance.

Figure 4-3. Clock Skew As Measured from Agent to Agent

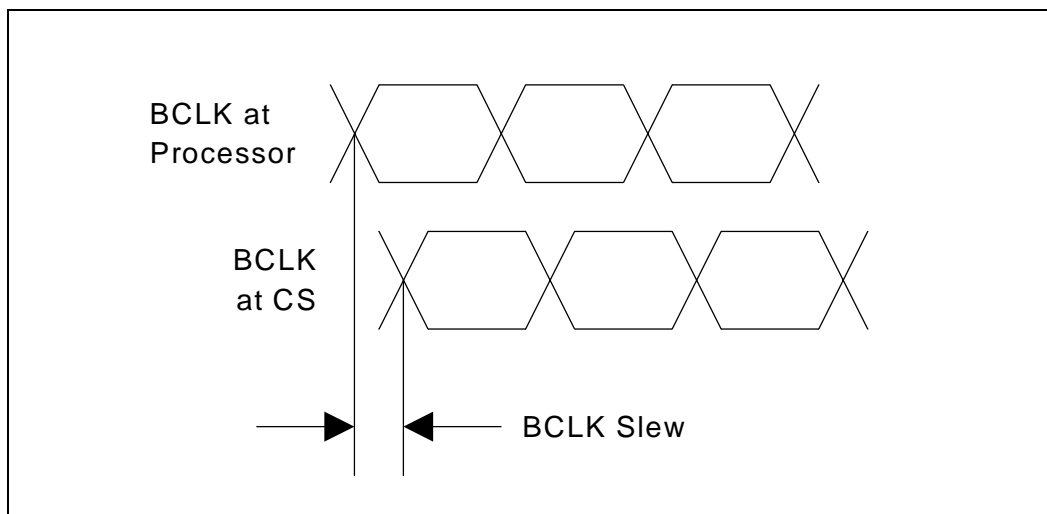
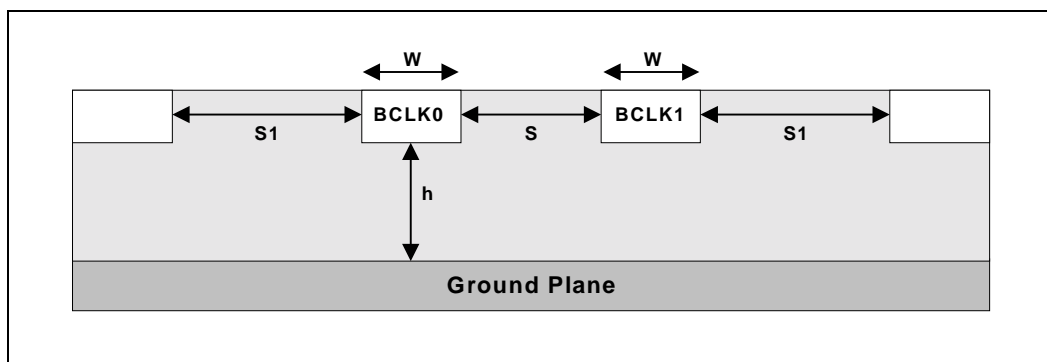


Figure 4-4. Trace Spacing for HOST\_CLK Clocks





### 4.1.1.2 HOST\_CLK General Routing Guidelines

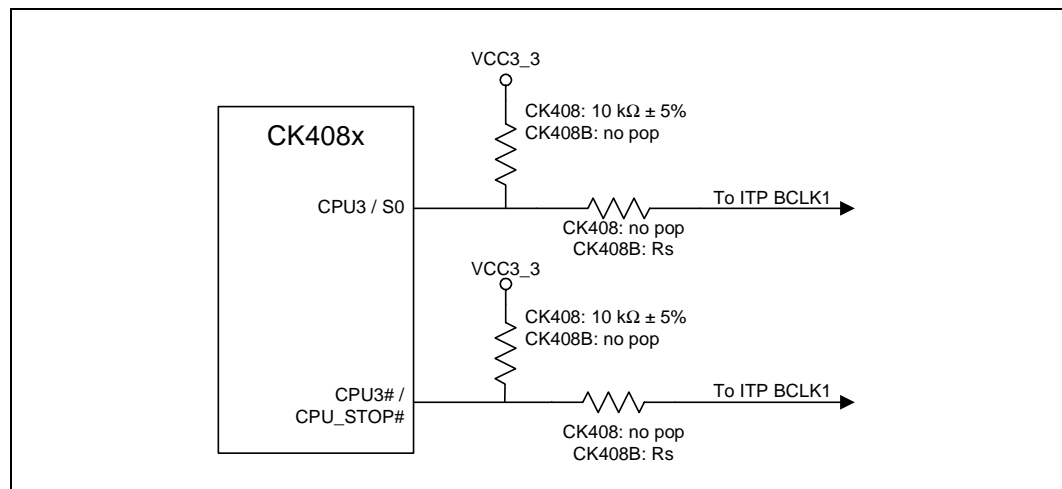
- When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers. Route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

### 4.1.1.3 CK408 vs. CK408B Requirement

The CK408 and CK408B are pin compatible. The only difference between the two chips is the CK408B replaces two signals on the CK408 with a fourth HOST\_CLK pair for the In\_Target\_Probe (ITP) and is preferred by board designers for preliminary testing and validation. While the CK408B pins need to be connected to the ITP, the CK408 pins require the following stuffing options:

- Add one  $10\text{ k}\Omega \pm 5\%$  pull-up resistor close to the clock driver before the  $33\text{ }\Omega \pm 5\%$  ( $R_s$ ) (see Figure 4-5) series resistor on each ITP signal trace (CPU3, CPU3#). This would give the option to use the CK408 instead of the CK408B.
- If deciding to go with CK408, having the  $33\text{ }\Omega \pm 5\%$  series resistor and  $49.9\text{ }\Omega \pm 1\%$  ( $R_t$ ) (see Figure 4-5) parallel resistor is not necessary.

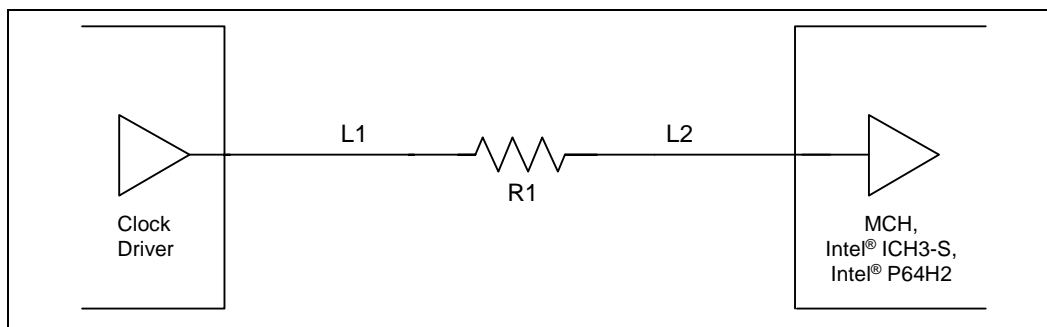
Figure 4-5. Stuffing Options for CK408 and CK408B



## 4.1.2 CLK66 Clock Group

In the CLK66 clock group, the driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, ICH3-S, and P64H2.

**Figure 4-6. Topology for CLK66**



**Table 4-4. CLK66 Routing Guidelines**

Parameters	Routing Guidelines
Clock Group	CLK66
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$50 \Omega \pm 10\%$
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00" – 0.50"
Trace Length – L2	3.00" – 9.0"
Resistor	$R1 = 43 \Omega \pm 5\%$
Skew Requirements	All the clocks in the CLK66 group must have < 100 mil skew between each other.
Clock Driver to MCH	$X = (3'' - 9.5'')^1$
Clock Driver to ICH3-S	$X = (3'' - 9.5'')$
Clock Driver to P64H2	$X - 0.34''^2$

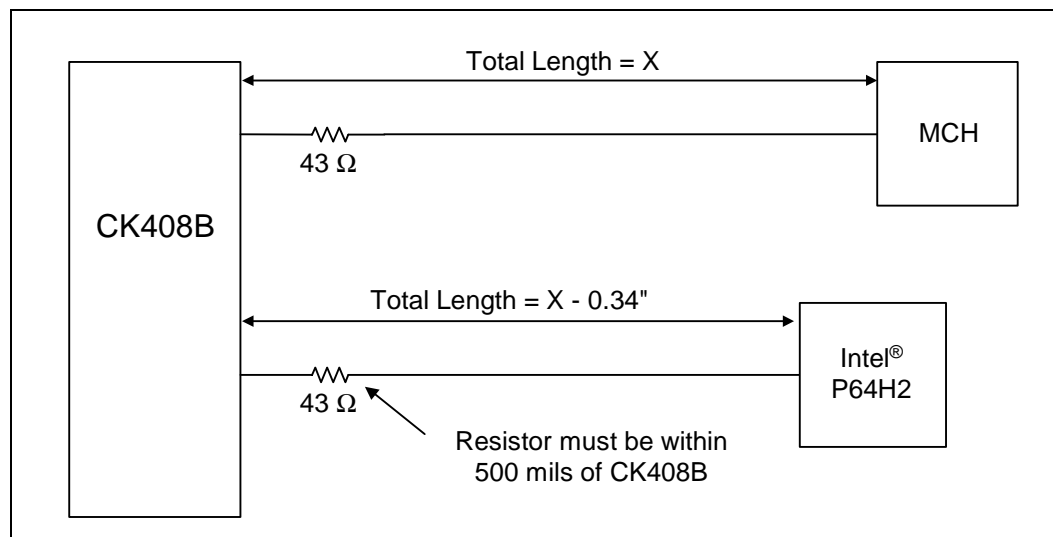
**NOTES:**

1. For better understanding of the concept, refer to [Section 4.1.2.1](#), [Figure 4-7](#) and [Figure 4-8](#).
2. Assuming no connector.

### 4.1.2.1 CLK66 Skew Requirements

Traces going to the P64H2 could have up to **two** connectors. Designers should keep in mind that all Total Lengths are referenced to the MCH length (“X”) and assume no connector. Each connector is equivalent to 0.60 inches of trace. Adding a single connector on the P64H2 trace would reduce the motherboard trace length by the card length “Z” to  $X - 0.34" - 0.60" - Z = X - 0.94" - Z$  (refer to Figure 4-8). In addition, some OEMs might consider having the components on a riser, in which case the riser card trace length designator “Y” should also be accounted for as yet another factor. In this case the last equation would become  $X - 0.34" - 0.60" - Z - 0.60" - Y = X - 1.54" - Y - Z$  (refer to Figure 4-9). Note that if a riser is used, the motherboard clock trace must be designed for the specific riser card trace length and connector.

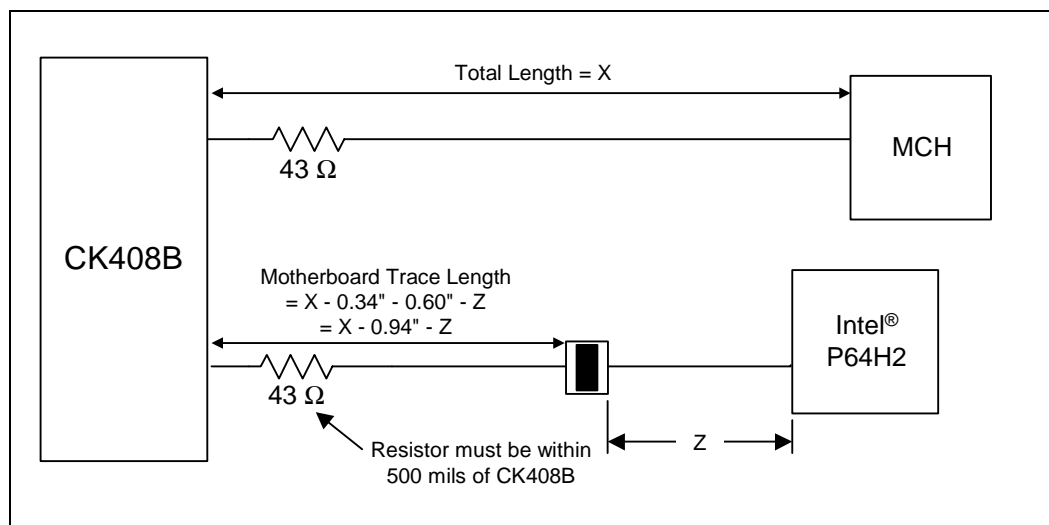
Figure 4-7. Clock Skew Requirements



**NOTES:**

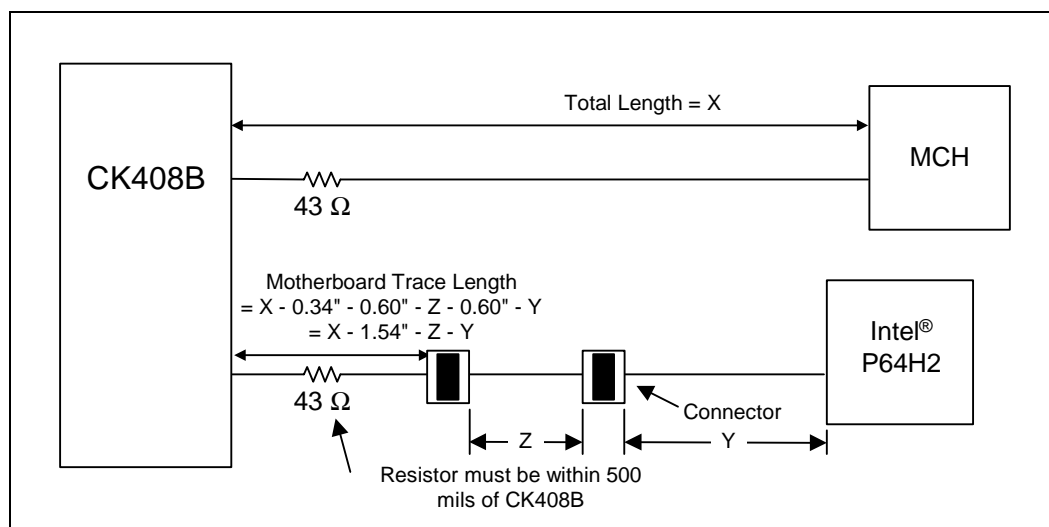
1. All lengths must be matched within 100 mils of target length.
2. 66 MHz clock lines routed with 25 mils isolation from any other signal.
3. Length from CK408B to MCH must be between 3" and 9.5".

Figure 4-8. Example of Adding a Single Connector

**NOTES:**

1. All lengths must be matched within 100 mils of target length.
2. 66 MHz clock lines routed with 25 mils isolation from any other signal.
3. Length from CK408B to MCH must be between 3" and 9.5".
4. Each connector is equivalent to  $\sim 0.60"$  of trace.
5.  $Z$  is the card trace length.

Figure 4-9. Example of Adding Two Connectors and/or a Riser

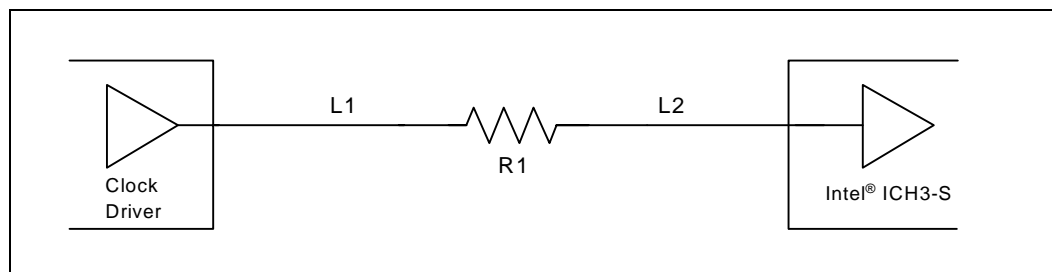
**NOTES:**

1. All lengths must be matched within 100 mils of target length.
2. 66 MHz clock lines routed with 25 mils isolation from any other signal.
3. Length from CK408B to MCH must be between 3" and 9.5".
4. Each connector is equivalent to  $\sim 0.60"$  of trace.
5. Each riser is equivalent to  $\sim 0.60" + Y$  where  $Y$  is the riser card trace length.
6. The riser must be built with the CLK66 trace length matched to the motherboard routed length.

### 4.1.3 CLK33\_ICH3-S Clock

In the CLK33\_ICH3-S case, the driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the ICH3-S.

**Figure 4-10. Topology for CLK33\_ICH3-S**



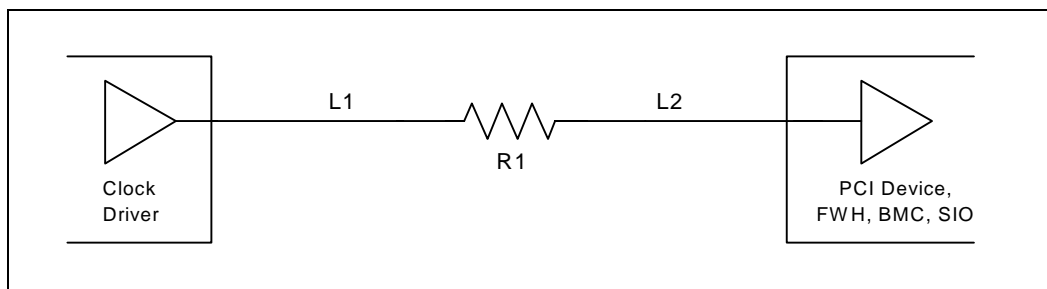
**Table 4-5. CLK33\_ICH3-S Routing Guidelines**

Parameter	Routing Guidelines
Clock Group	CLK33_ICH3-S
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$50\ \Omega \pm 10\%$
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00" – 0.50"
Trace Length – L2	3.00" – 9.0"
Resistor	$R1 = 33\ \Omega \pm 5\%$
Skew Requirements	Must be matched to $\pm 100$ mils of CLK66

#### 4.1.4 CLK33 Clock Group

For the CLK33 clock group, the driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the PCI devices on the PCI cards.

**Figure 4-11. Topology for CLK33 to PCI Device Down**



**Table 4-6. CLK33 Routing Guidelines for PCI Device Down**

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$50\ \Omega \pm 10\%$
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00" – 0.50"
Trace Length – L2	3.00" – 9.0"
Resistor	$R1 = 33\ \Omega \pm 5\%$
Skew Requirements	PCI device – PCI device skew max allowed by <i>PCI Local Bus Specification, Rev 2.2</i> is 2 ns. Therefore, length match with other CLK33 signals within $\pm 1$ ns.

Figure 4-12. Topology for CLK33 to PCI Slot

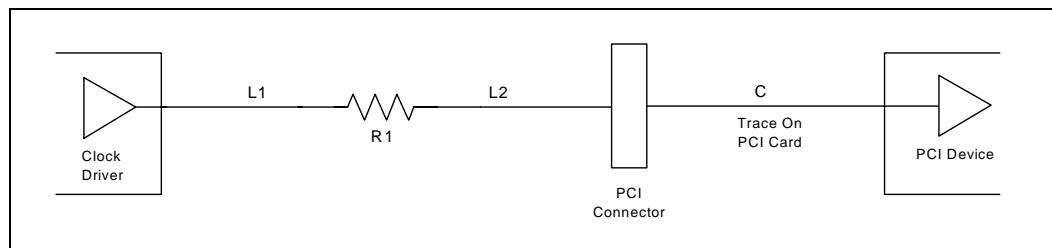


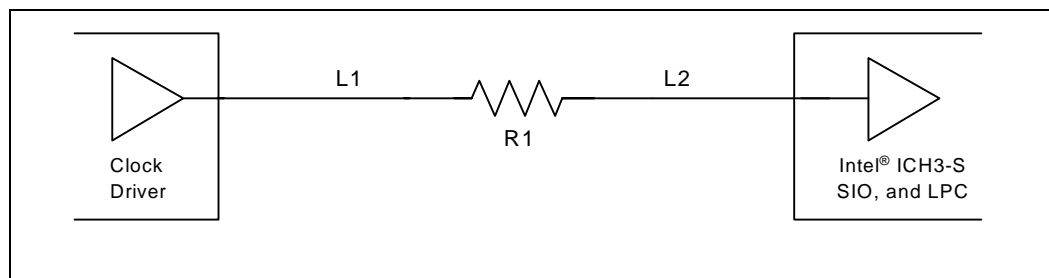
Table 4-7. CLK33 Routing Guidelines for PCI Slot

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$50 \Omega \pm 10\%$
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0.00" – 0.50"
Trace Length – L2	3.00" – 9.0"
Trace Length – C	Routed 2.50" per <i>PCI Local Bus Specification, Rev 2.2</i>
Resistor	$R1 = 33 \Omega \pm 5\%$
Skew Requirements	PCI device – PCI device skew max allowed by <i>PCI Local Bus Specification, Rev 2.2</i> is 2 ns. Therefore, length match with other CLK33 signals within $\pm 1$ ns.
Maximum Via Count Per Signal	1

## 4.1.5 CLK14 Clock Group

The driver in the CLK14 clock group is the clock synthesizer 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the ICH3-S, SIO and LPC.

**Figure 4-13. Topology for CLK14**



**Table 4-8. CLK14 Routing Guidelines**

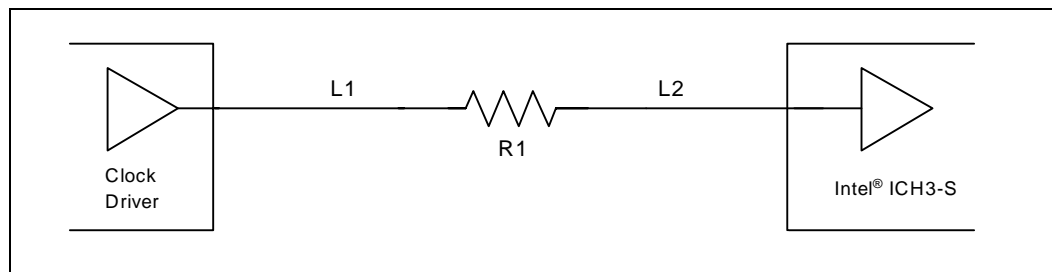
Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$50\ \Omega \pm 10\%$
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0.00" – 0.50"
Trace Length – L2	3.00" – 9.0"
Resistor	$R1 = 22\ \Omega \pm 5\%$
Skew Requirements	None



### 4.1.6 USBCLK Clock Group

For the USBCLK clock group, the driver is the clock synthesizer USB clock output buffer, and the receiver is the USB clock input buffer at the ICH3-S. Note that this clock is asynchronous to any other clock on the board.

**Figure 4-14. Topology for USB\_CLK**



**Table 4-9. USBCLK Routing Guidelines**

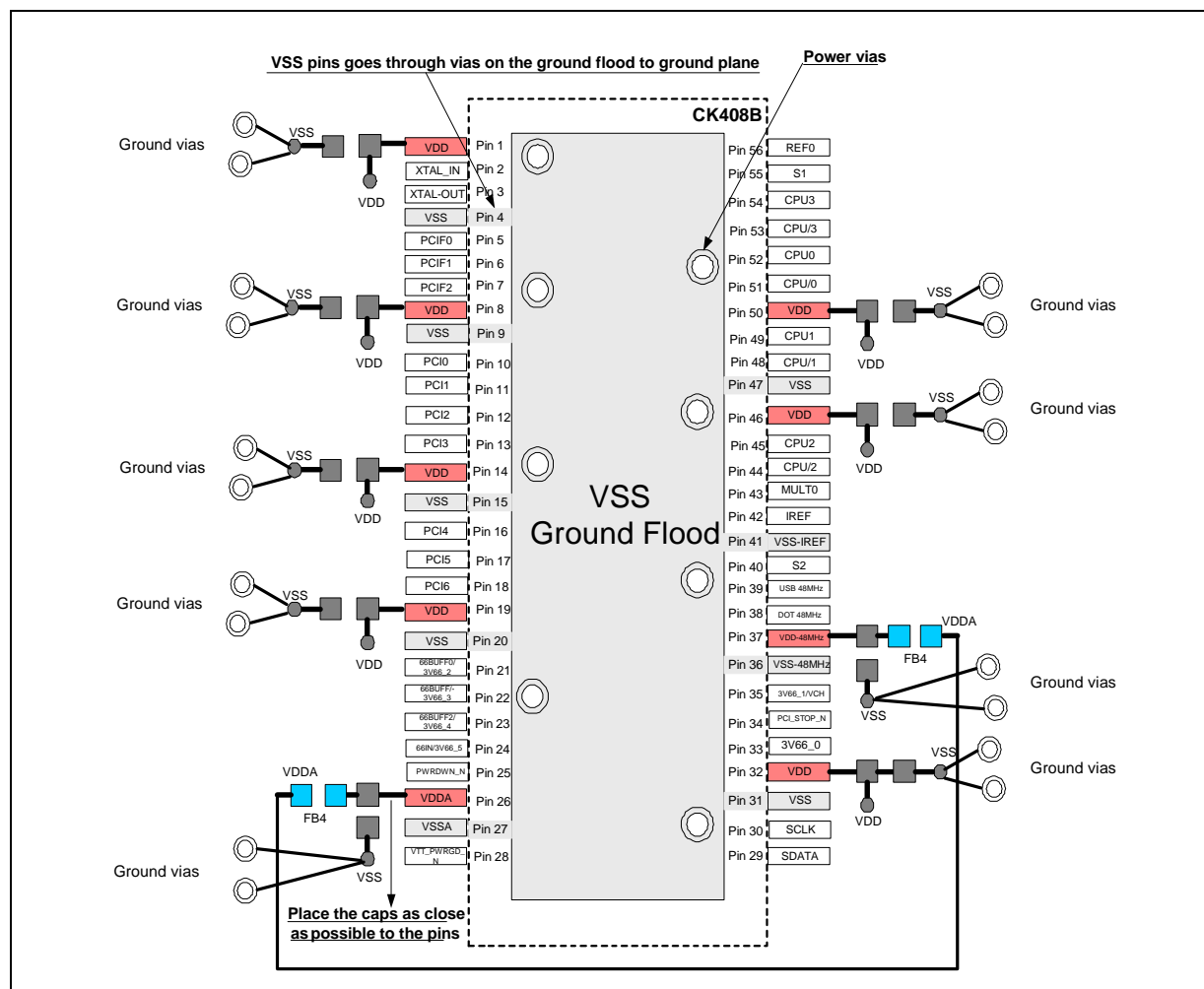
Parameter	Routing Guideline
Clock Group	USBCLK
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance ( $Z_0$ )	$50\ \Omega \pm 10\%$
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00" – 0.50"
Trace Length – L2	3.00" – 12.00"
Resistor	$R1 = 33\ \Omega \pm 5\%$
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board
Maximum Via Count	2

## 4.2 Clock Driver Decoupling

The decoupling requirements for a CK408B compliant clock synthesizer are as follows:

- One, 22  $\mu$ F polarized (decoupling) capacitor placed close to the VDD generation circuitry.
- Eleven, 0.1  $\mu$ F high-frequency decoupling capacitors placed close to the VDD pins on the clock driver.
- Three, 0.1  $\mu$ F high-frequency decoupling capacitors placed close to the VDDA pins on the clock driver.
- One, 10  $\mu$ F polarized (decoupling) capacitor placed close to the VDDA pins on the clock driver.
- One, 0.1  $\mu$ F high-frequency decoupling capacitor placed close to the VDDA generation circuitry.
- All decoupling capacitors should be placed close to the clock driver pins. Refer to [Figure 4-15](#).

**Figure 4-15. Decoupling Capacitors Placement and Connectivity**



## 4.3 Clock Driver Power Delivery

Designers must take special care to provide a quiet VDDA supply to the Ref VDD, VDDA and the 48 MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the clock chip. They are also sensitive to switching noise generated elsewhere in the system such as the processor voltage regulator. It is recommended that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins. In addition, power vias should be distributed evenly throughout the ground flood.

**Note:** For all power connections to planes, decoupling capacitors, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.

## 4.4 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.
- Turn off all unused clocks.

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# System Bus Routing Guidelines 5

This section covers the system bus source synchronous (data, address, and associated strobes) and common clock signal routing. [Table 5-1](#) lists the signals and their corresponding signal types.

**Table 5-1. System Bus Signal Groups**

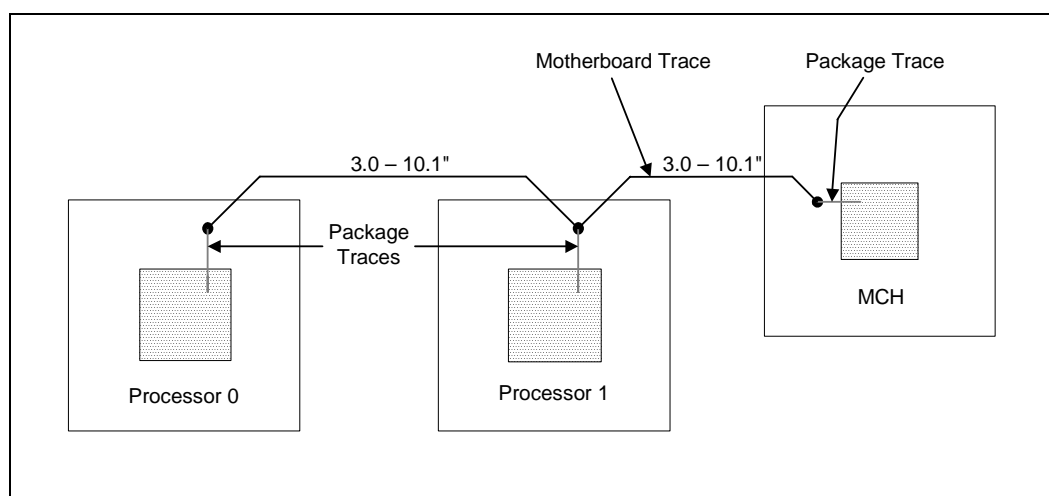
Signal Group	Type	Signals
AGTL+ Common Clock Input	Synchronous to BCLK	BPRI#, BR[3:1]# <sup>1,2</sup> , DEFER#, RESET# <sup>1</sup> , RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK	ADS#, AP[1:0]#, BINIT# <sup>3</sup> , BNR# <sup>3</sup> , BPM[5:0]# <sup>1</sup> , BR0# <sup>1</sup> , DBSY#, DP[3:0]#, DRDY#, HIT# <sup>3</sup> , HITM# <sup>3</sup> , LOCK#, MCERR# <sup>3</sup>
AGTL+ Source Synchronous I/O: 4X Group	Synchronous to assoc. strobe	D[63:0]#, DBI[3:0]#
AGTL+ Source Synchronous I/O: 2X Group	Synchronous to assoc. strobe	A[35:3]# <sup>4</sup> , REQ[4:0]#
AGTL+ Strobes	Synchronous to BCLK [1:0]	ADSTB[1:0]#, DSTBN[3:0]#, DSTBP[3:0]#
Async GTL+ Input <sup>1</sup>	Asynchronous	A20M#, IGNNE#, INIT# <sup>4</sup> , LINT0/INTR, LINT1/ NMI, PWRGOOD, SMI# <sup>4</sup> , CPUSLP#, STPCLK#
Async GTL+ Output <sup>1</sup>	Asynchronous	FERR#, IERR#, PROCHOT#, THERMTRIP#
System Bus Clock	Clock	BCLK0, BCLK1
TAP Input <sup>6</sup>	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output <sup>6</sup>	Synchronous to TCK	TDO
SMBus Interface <sup>1</sup>	Synchronous to SM_CLK	SM_EP_A[2:0], SM_TS_A[1:0], SM_DAT, SM_CLK, SM_ALERT#, SM_WP
Power/Other	Power/Other	GTLREF[3:0], COMP[1:0], ODTEN, RESERVED, SKTOCC#, TESTHI[6:0], VID[4:0], VCC_CPU, SM_VCC <sup>5</sup> , VCCA, VSSA, VCCIOPLL, VSS, VCCSENSE, VSSSENSE

**NOTES:**

1. These signals do not have on-die termination on the processor. They must be terminated properly on the motherboard. If the signal is not connected, it must be pulled to the appropriate voltage level through a  $1\text{ k}\Omega \pm 5\%$  resistor.
2. Xeon processors use only BR0# and BR1#.
3. These signals are 'wired-OR' signals and may be driven simultaneously by multiple agents. For further details on how to implement wired-OR signals, refer to the routing guidelines in [Section 5.2.1](#).
4. The value of these pins during the active edge of RESET# determine processor configuration options.
5. SM\_VCC has critical power sequencing requirements.
6. Terminations and routing for TAP signals and all debug port signals are found in the *ITP700 Debug Port Design Guide*.

The dual processor topology requires that the MCH be at one end of the bus, Processor 0 be at the other end of the bus, and Processor 1 be in the middle of the bus ([Figure 5-1](#)). The motherboard routing to Processor 1 must not create a stub on the system bus signals at the socket. This requires routing into the socket and back out of the socket. For UP operation, the single processor must be installed in the Processor 0 socket, at the end of the bus. [Figure 5-1](#) shows the recommended dual processor topology used for system bus routing.

**Figure 5-1. Dual Processor System Bus Topology**



Refer to [Table 5-2](#) for a summary of the dual processor system bus routing recommendations. Use this as a quick reference only. The following sections provide more detailed information for each parameter. Intel strongly recommends simulation of all signals to ensure the design meets setup and hold times.

**Table 5-2. System Bus Routing Summary**

Parameter	Platform Routing Guidelines
Trace Width/Spacing	5/15 mils.
2X and 4X Signal Group Line Lengths (Agent-to-Agent Length)	3.0" – 10.1" pin-to-pin. Total bus length must not exceed 20.2". Trace lengths must be balanced $\pm 25$ mils with respect to the strobe between agents to compensate for the stub created by the processor package.
DSTBN3[:0]# / DSTBP[3:0]# and ADSTB[1:0]# Line Lengths	Should follow the same routing rules as the 2X and 4X Signal Group. A 25 mil spacing should be maintained around each strobe signal. Do not route differentially.
Common Clock Signal Line Lengths	Common Clock signals should follow the same routing rules as the Data signals, however no length compensation is necessary.
Topology	Daisy chain with the chipset at one end of the system bus and Processor 0 at the other. End processor must have on-die termination enabled.
Routing Requirements	No motherboard contribution to stub length of middle processor (< 35 mil trace from via to pad). All signals within the same strobe group must be routed on same layer for entire length of bus.
Reference Plane Requirements	Ground referenced only. Avoid changing layers when routing system bus signals. If a layer change must occur, use vias connecting the two reference planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via. For 2X and 4X signals, ADSTB[1:0]#, and DSTBN3[:0]# / DSTBP[3:0]#: NEVER ROUTE OVER A PLANE SPLIT.
Motherboard Impedance	50 $\Omega \pm 10\%$ .

## 5.1 Routing Guidelines for the AGTL+ Source Synchronous 2X and 4X Groups

The 4X group of signals uses four times the frequency of the base clock, or 400 MHz. The 2X group uses twice the frequency of the base clock, or 200 MHz. The 2X and 4X signals are listed in Table 5-3. Table 5-4 lists the 2X and 4X signals with their associated strobes.

**Table 5-3. 2X and 4X Signal Groups**

2X Group	4X Group
A[35:3]# REQ[4:0]#	HD[63:0]# DBI[3:0]#

**Table 5-4. Source Synchronous Signals with the Associated Strobes**

Signals	Associated Strobe
REQ[4:0]#, HA[16:3]#	ADSTB0#
A[35:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Routing guidelines for the 2X and 4X signal groups are given in Table 5-2. All 2X and 4X signals of the same group (refer to Table 5-4) must be routed within  $\pm 25$  mils of the same length between agents and within  $\pm 50$  mils of the entire length of the bus.

### 5.1.1 Trace Length Matching

Trace length matching is required within each source synchronous group to compensate for the package trace length differences between data signals and the associated strobe. This balances the strobe-to-signal skew in the middle of the setup and hold window. Additional compensation must be added to account for the capacitive loading effects of the processor socket stubs. Figure 5-2 shows how to implement trace length matching. An example of trace length matching is given in Example on page 5-57.

Trace length matching consists of matching the pad-to-pad lengths for every signal within a signal group (e.g., A[35:17]# and ADSTB1#). A pad-to-pad length is measured as follows:

$$\text{CPU}_{\text{pad-to-CPU}_{\text{pad}}} = \text{CPU0}_{\text{pkg\_len}} + \text{CPU}_{\text{pin-to-CPU}_{\text{pin}}} + \text{CPU1}_{\text{pkg\_comp}}$$

$$\text{CPU}_{\text{pad-to-MCH}_{\text{pad}}} = \text{CPU1}_{\text{pkg\_comp}} + \text{CPU}_{\text{pin-to-MCH}_{\text{pin}}} + \text{MCH}_{\text{pkg\_len}}$$

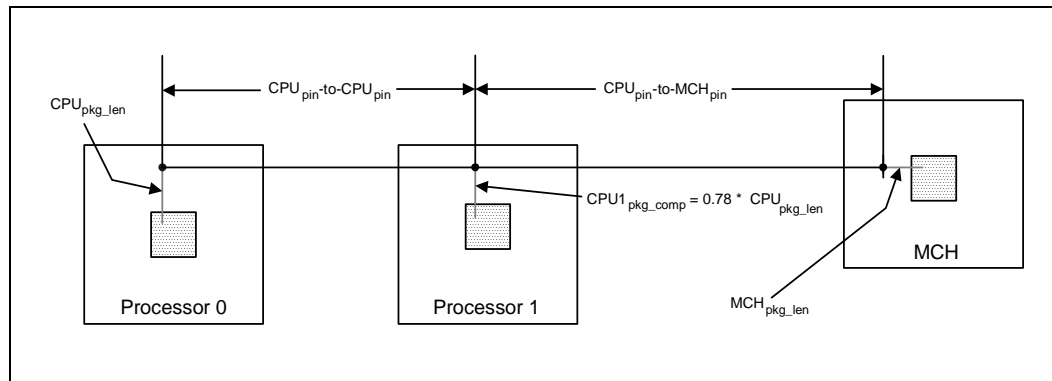
Where:

- $\text{CPU}_{\text{pin-to-CPU}_{\text{pin}}}$  = Motherboard trace length between Processor 0 and Processor 1.
- $\text{CPU}_{\text{pin-to-MCH}_{\text{pin}}}$  = Motherboard trace length between Processor 1 and MCH.
- $\text{pkg\_len}$  = Pad to pin length within the package.
- 0.78 = Compensation due to capacitive loading of processor 1 socket.
- $\text{CPU1}_{\text{pkg\_comp}}$  =  $\text{CPU}_{\text{pkg\_len}} * (\text{capacitive loading compensation})$
- =  $\text{CPU}_{\text{pkg\_len}} * 0.78$



The package trace lengths for the MCH are available in the *Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet*. The package trace lengths for the Intel Xeon processor with 512 KB L2 cache are available in the matching spreadsheet contained in the *Intel® Xeon™ Processor with 512 Cache Signal Integrity Models*.

**Figure 5-2. Trace Length Matching for the Dual Processor System Bus**



When length matching, every signal's pad to pad length is set equal to each other ( $\pm 25$  mils). This yields the following equation:

$$\begin{aligned} \text{CPU0}_{\text{pkg\_len}}(\text{Signal 1}) + \text{CPU}_{\text{pad-to-CPU}_{\text{pad}}}(\text{Signal 1}) + 0.78 * \text{CPU1}_{\text{pkg\_len}}(\text{Signal 1}) = \\ \text{CPU0}_{\text{pkg\_len}}(\text{Signal 2}) + \text{CPU}_{\text{pad-to-CPU}_{\text{pad}}}(\text{Signal 2}) + 0.78 * \text{CPU1}_{\text{pkg\_len}}(\text{Signal 2}) \end{aligned}$$

To length match Signal 1 and Signal 2, hold one of the signals constant, and vary the second signal until the equation is satisfied. Since all the  $\text{pkg\_len}$  values are constant, we can solve for Signal 2:

$$\begin{aligned} \text{CPU}_{\text{pad-to-CPU}_{\text{pad}}}(\text{Signal 2}) = \text{CPU0}_{\text{pkg\_len}}(\text{Signal 1}) + \text{CPU}_{\text{pad-to-CPU}_{\text{pad}}}(\text{Signal 1}) \\ + 0.78 * \text{CPU1}_{\text{pkg\_len}}(\text{Signal 1}) - \text{CPU0}_{\text{pkg\_len}}(\text{Signal 2}) - 0.78 * \text{CPU1}_{\text{pkg\_len}}(\text{Signal 2}) \end{aligned}$$

Generally, when length matching a group of signals, a designer will first layout all signals to the shortest length possible allowed by specification. Then, keeping the longest signal as the constant value (Signal 1), lengthen all the other signals so that the pad to pad lengths are all equal.

### Trace Length Matching Example

Consider two signals, DSTBP0 and HD4, from the same group. Assume a nominal PCB length of 4.00". Calculate CPU to CPU length:

$$\text{CPU}_{\text{pin-to-CPU}_{\text{pin}}}(\text{HD4}) (\text{motherboard trace from Processor 0 to Processor 1}) = 4.000"$$

$$\text{CPU}_{\text{pkg\_len}}(\text{DSTBP0}) (\text{strobe package trace length}) = 0.150"$$

$$\text{CPU}_{\text{pkg\_len}}(\text{HD4}) (\text{HD4 package trace length}) = 0.350"$$

$$\text{CPU1}_{\text{pkg\_comp}}(\text{DSTBP0}) = 0.78 * \text{CPU}_{\text{pkg\_len}}(\text{DSTBP0}) = 0.78 * 0.150" = 0.117"$$

$$\text{CPU1}_{\text{pkg\_comp}}(\text{HD4}) = 0.78 * \text{CPU}_{\text{pkg\_len}}(\text{HD4}) = 0.78 * 0.350" = 0.273"$$

$$\begin{aligned} \text{CPU}_{\text{pin-to-CPU}_{\text{pin}}}(\text{DSTBP0}) &= \text{CPU}_{\text{pkg\_len}}(\text{HD4}) + \text{CPU}_{\text{pin-to-CPU}_{\text{pin}}}(\text{HD4}) \\ &+ \text{CPU1}_{\text{pkg\_comp}}(\text{HD4}) - \text{CPU}_{\text{pkg\_len}}(\text{DSTBP0}) - \text{CPU1}_{\text{pkg\_comp}}(\text{DSTBP0}) \\ &= 0.350 + 4.000 + 0.273 - 0.150 - 0.117 \end{aligned}$$

$$\text{CPU}_{\text{pin-to-CPU}_{\text{pin}}}(\text{DSTBP0}) = 4.356"$$

Therefore, the PCB trace length of DSTBP0 must be within  $\pm 25$  mils of 4.356" from Processor 0 to Processor 1.

Calculate CPU to MCH length assuming the CPU to MCH PCB length to be 9.0":

$$\text{CPU}_{\text{pin-to-MCH}_{\text{pin}}}(\text{HD4}) \text{ (motherboard trace from Processor 0 to Processor 1)} = 9.000"$$

$$\text{MCH}_{\text{pkg\_len}}(\text{DSTBP0}) \text{ (strobe package trace length)} = 0.190"$$

$$\text{MCH}_{\text{pkg\_len}}(\text{HD4}) \text{ (HD4 package trace length)} = 0.280"$$

$$\text{CPU1}_{\text{pkg\_comp}}(\text{DSTBP0}) = 0.78 * \text{CPU}_{\text{pkg\_len}}(\text{DSTBP0}) = 0.78 * 0.150" = 0.117"$$

$$\text{CPU1}_{\text{pkg\_comp}}(\text{HD4}) = 0.78 * \text{CPU1}_{\text{pkg\_len}}(\text{HD4}) = 0.78 * 0.350" = 0.273"$$

$$\begin{aligned} \text{CPU}_{\text{pin-to-MCH}_{\text{pin}}}(\text{DSTBP0}) &= \text{MCH}_{\text{pkg\_len}}(\text{HD4}) + \text{CPU}_{\text{pin-to-MCH}_{\text{pin}}}(\text{HD4}) \\ &\quad + \text{CPU1}_{\text{pkg\_comp}}(\text{HD4}) - \text{MCH}_{\text{pkg\_len}}(\text{DSTBP0}) - \text{CPU1}_{\text{pkg\_comp}}(\text{DSTBP0}) \\ &= 0.280 + 9.000 + 0.273 - 0.190 - 0.117 \end{aligned}$$

$$\text{CPU}_{\text{pin-to-MCH}_{\text{pin}}}(\text{DSTBP0}) = 9.246"$$

Therefore, the PCB trace length of DSTBP0 must be within  $\pm 25$  mils of 9.246" from Processor 1 to the MCH.

## 5.2 Routing Guidelines for Common Clock Signals

Table 5-5 lists the Common clock signals.

**Table 5-5. AGTL+ Common Clock I/O Signals**

Signal Types	Signals
Input	BPRI#, BR[3:1]#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
I/O	ADS#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#

Route the common clock signals according to the processor system bus topology shown in Figure 5-1. Routing guidelines for the common clock signal group are in Table 5-2. Route the traces with at least 50% of the trace width directly over a reference plane.

### 5.2.1 Wired-OR Signals

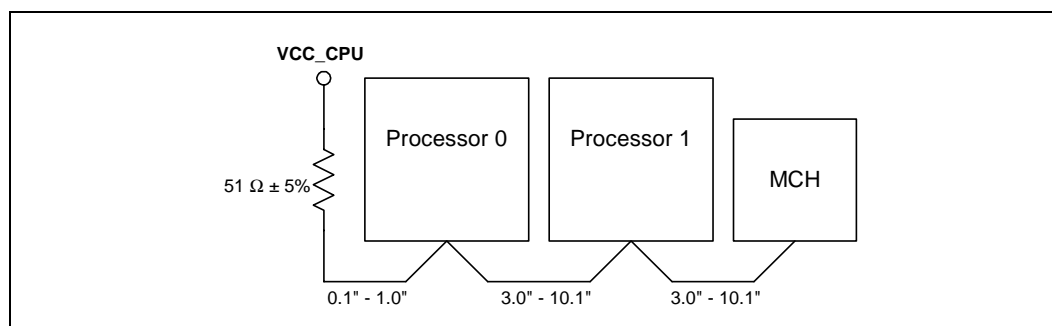
There are five “wired-OR” signals on the system bus. These signals are HIT#, HITM#, MCERR#, BINIT#, and BNR#. These signals differ from the other system bus signals in that more than one agent can be driving the signal at the same time. However, Intel recommends that special attention be given to the routing of these signals in adherence to the layout guidelines presented in Table 5-2. Timing and signal integrity must be met for the cases where one agent is driving, all agents are driving, and any combination of agents are driving.

The wired-OR signals should follow the same routing rules as the common clock signals. Intel recommends that simulations for these signals be performed for each system.

## 5.2.2 RESET# Topology

Since the processor does not contain on-die termination for the RESET# input signal, these additional layout guidelines for the RESET# signal are required. The baseboard trace length from Processor 0's pin to the termination resistor should be 0 to 1 inch. Follow the same routing guidelines given for common clock signals listed above in this same section.

**Figure 5-3. RESET# Topology**



## 5.3 Routing Guidelines for Asynchronous GTL+ and Miscellaneous Signals

Table 5-6 enumerates the remainder of the processor signals discussed in this document.

**Table 5-6. Asynchronous GTL+ and Miscellaneous Signals (Sheet 1 of 2)**

Signal Name	Type	Processor I/O Type	Driven By	Received By
A20M#	Async GTL+	I	ICH3-S	Processor
BINIT#	AGTL+	I/O	Processor	Processor
BR[3:1]#	AGTL+	I	Processor	Processor
BR0#	AGTL+	I/O	Processor/MCH	Processor/MCH
COMP[1:0]	Analog	I	Pull-down	Processor
FERR#	Async GTL+	O	Processor	ICH3-S
IERR#	Async GTL+	O	Processor	External Logic (such as Baseboard Management Controller)
IGNNE#	Async GTL+	I	ICH3-S	Processor
INIT#	Async GTL+	I	ICH3-S	Processor
LINT[1:0]	Async GTL+	I	ICH3-S	Processor
ODTEN	Other	I	Pull-up / Pull-down	Processor
PROCHOT#	Async GTL+	O	Processor	External Logic
PWRGOOD	Async GTL+	I	External Logic	Processor
SLP#	Async GTL+	I	ICH3-S	Processor
SM_ALERT#	SMBUS (3.3 V)	O	Processor/Controller	Controller
SM_CLK	SMBUS (3.3 V)	I/O	Processor/Controller	Processor/Controller

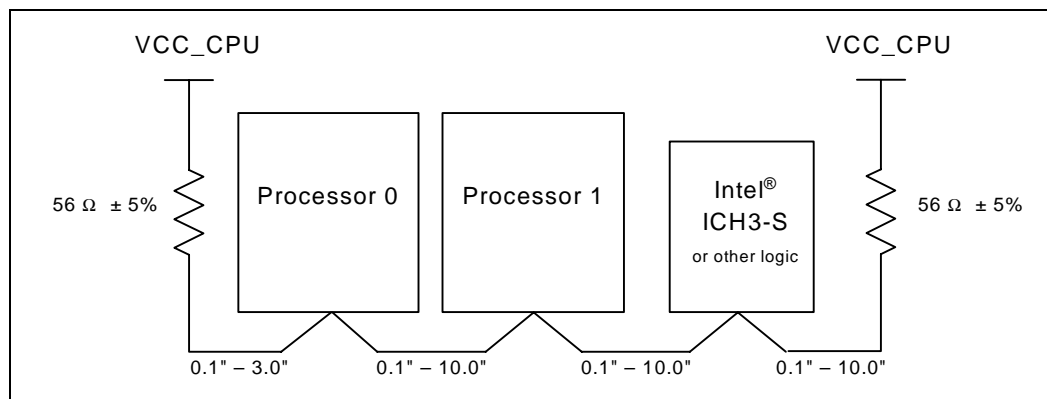
Table 5-6. Asynchronous GTL+ and Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Type	Processor I/O Type	Driven By	Received By
SM_DAT	SMBUS (3.3 V)	I/O	Processor/Controller	Processor/Controller
SM_EP_A[2:0]	SMBUS (3.3 V)	I	Pull-up / Pull-down	Processor
SM_TS_A[1:0]	SMBUS (3.3 V)	I	Pull-up / Pull-down	Processor
SM_WP	SMBUS (3.3 V)	I	External Logic	Processor
SMI#	Async GTL+	I	ICH3-S	Processor
STPCLK#	Async GTL+	I	ICH3-S	Processor
THERMTRIP#	Async GTL+	O	Processor	External Logic
VCCA	Power	I	Pull-up / Pull-down	Processor
VCCIOPLL	Power	I	Pull-up / Pull-down	Processor
VCCSENSE	Other	O	Processor	Voltage Regulator
VID[4:0]	Other	O	Processor	Voltage Regulator
GTLREF	Power	I	Pull-up / Pull-down	Processor
VSSA	Power	I	Pull-up / Pull-down	Processor
VSSSENSE	Other	O	Processor	Voltage Regulator

### 5.3.1 Asynchronous GTL+ Signals Driven by the Processor

Follow the topology shown in Figure 5-4 when routing FERR#, IERR#, PROCHOT# and THERMTRIP#. Note that FERR# is the only signal in this group that connects the processors to the ICH3-S. IERR#, PROCHOT# and THERMTRIP# connect to other motherboard logic (such as the Baseboard Management Controller) and may need voltage translation logic, depending on the motherboard receiver logic devices used. Do not route a stub when routing to the processors.

Figure 5-4. Topology for Asynchronous GTL+ Signals Driven by the Processor



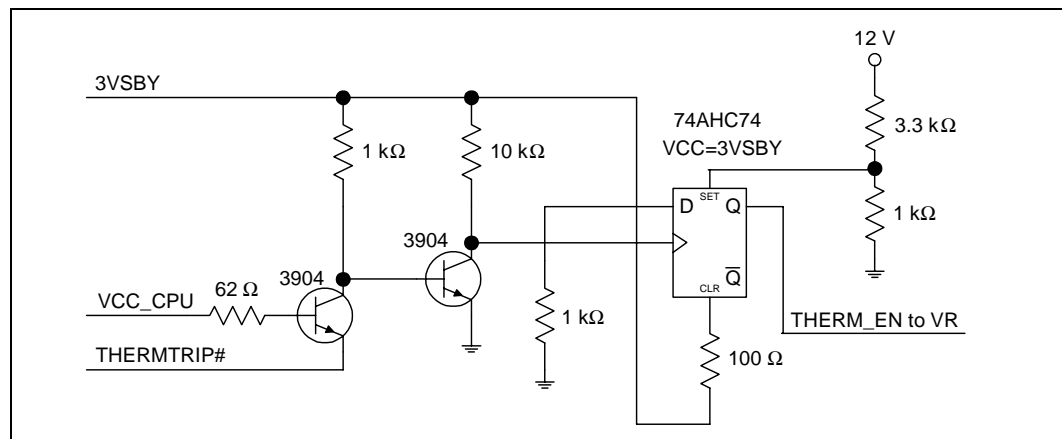
**NOTES:**

1. Trace  $Z_0 = 50 \Omega$ .
2. Trace spacing = 10 mil.

### 5.3.1.1 Proper THERMTRIP# Usage

To protect the processors from damage in over-temperature situations, power to the processor core must be removed within 0.5 seconds of the assertion of THERMTRIP#. If power is applied to a processor when no thermal solution is attached, normal leakage currents causes the die temperature to rapidly rise to levels at which permanent silicon damage is possible. This high temperature causes THERMTRIP# to go active. Use dual termination on the THERMTRIP# signal. Each processor's THERMTRIP# can be routed to its own receiver, or they can be wire-OR'd together. If routed separately, each signal must be terminated at the receiver end only. All power supply sources to all processors must be disabled when any installed processor signals THERMTRIP#. In the reference schematic, the 74AHC74 flip-flop latches the THERMTRIP# signal HIGH after a PWRGOOD assertion, and LOW after a THERMTRIP# assertion.

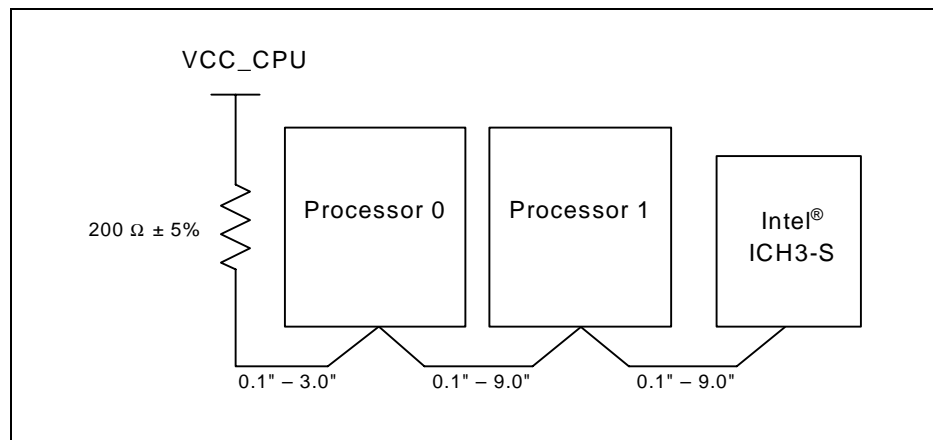
Figure 5-5. Recommended THERMTRIP# Circuit



### 5.3.2 Asynchronous GTL+ Signals Driven by the Chipset

Follow the topology shown in Figure 5-6 when routing A20M#, IGNNE#, INIT#, LINT[1:0], CPUSLP#, SMI# and STPCLK#. Do not route a stub when routing to the processors.

Figure 5-6. Topology for Asynchronous GTL+ Signals Driven by the Chipset



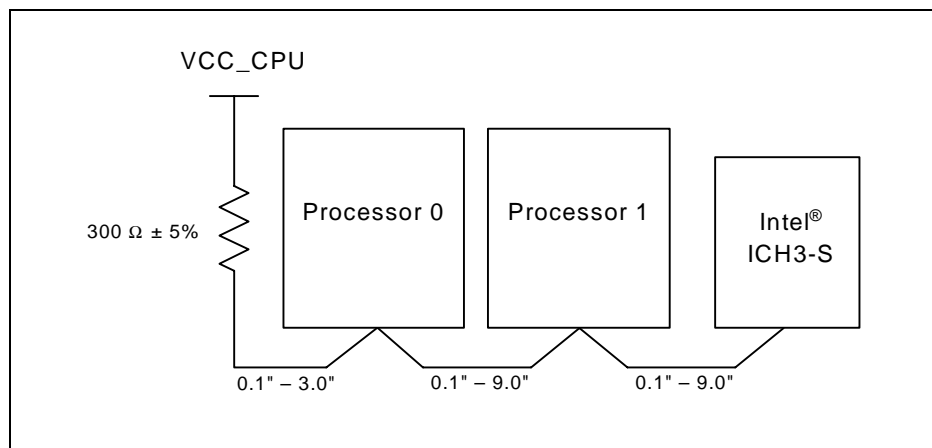
**NOTES:**

1. Trace  $Z_0 = 50 \Omega$ .
2. Trace spacing = 10 mil.

### 5.3.2.1 Proper Power Good Usage

Route CPUPWRGD as shown in Figure 5-7. You may choose to isolate PWRGOOD for each voltage regulator and processor pair in order to recognize individual voltage regulator failures.

Figure 5-7. Topology for PWRGOOD (CPUPWRGOOD)



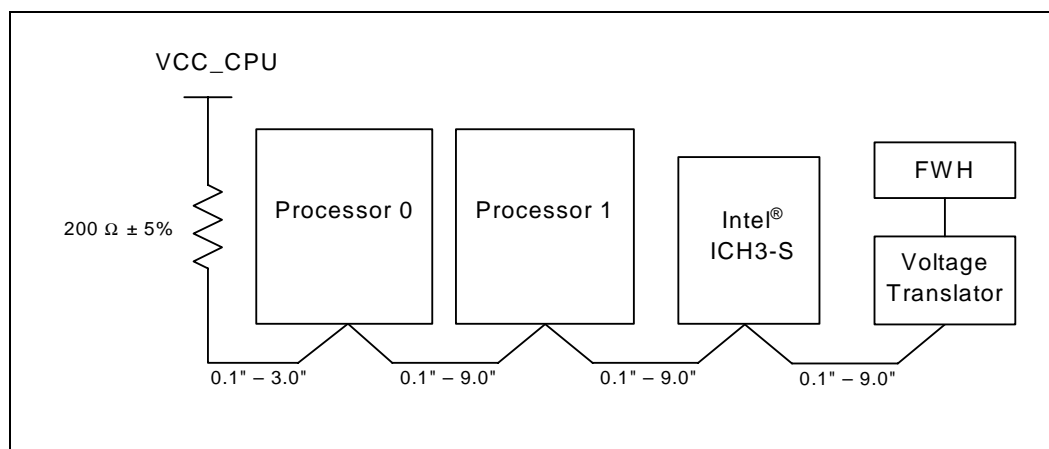
**NOTES:**

1. Trace  $Z_0 = 50 \Omega$ .
2. Trace spacing = 10 mil.

### 5.3.2.2 Voltage Translation for INIT#

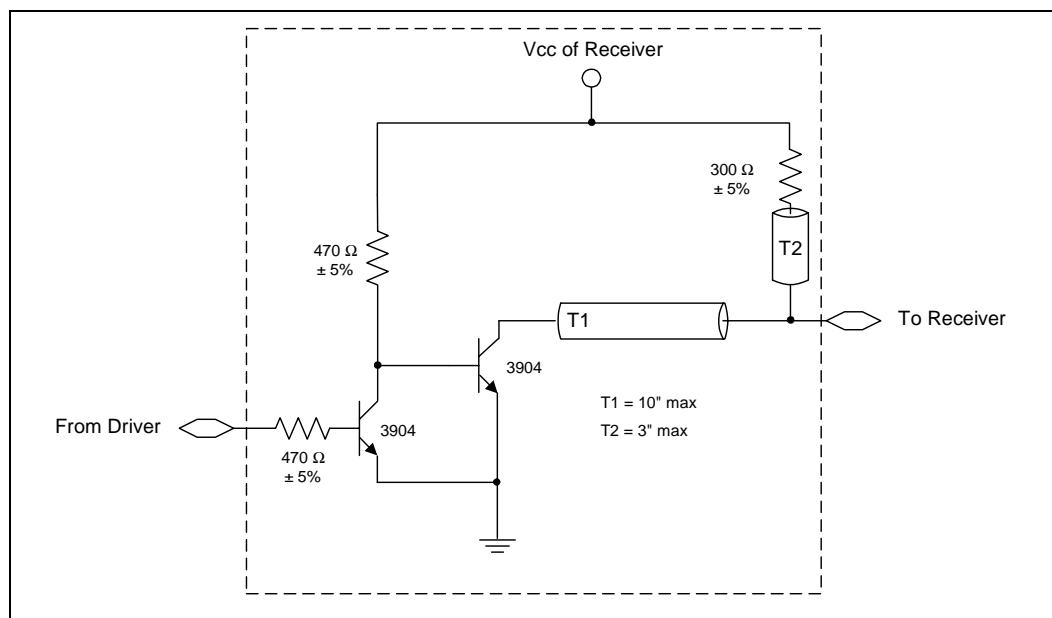
A voltage translator circuit is required for the INIT# signal for all platforms that use the FWH. The required routing topology for INIT# is given in Figure 5-8. Do not route a stub when routing to the processors. Figure 5-9 shows the voltage translator circuit.

Figure 5-8. INIT# Routing Topology



**NOTE:** The total trace length between the ICH3-S pin and the Processor 0 pin must be less than 15 inches.

Figure 5-9. Voltage Translator Circuit



**NOTE:** T1 and T2 must be referenced to ground.

### 5.3.3 VID[4:0]

Route the VID[4:0] signals of the processor to the VID[4:0] inputs of the voltage regulator controller. The voltage regulator controller should provide internal pull-up resistors for these signals. Refer to the *VRM 9.1 DC-DC Converter Design Guidelines* and the specification of the voltage controller specific to your design for further details.

Since both processors must operate at the same voltage, the designer should provide a way to check the VID[4:0] signals to ensure a processor does not operate out of specification. (Refer to [Figure 12-3](#) for more information.)

### 5.3.4 SMBus Signals

The SMBus signals provide access to the thermal sensor and memory device on the processor. The signaling protocol used adheres to the specification of the System Management Bus. Refer to *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet* for details on the Xeon processor implementation and addressing scheme.

Connect the SM\_ALERT#, SM\_CLK, and SM\_DAT signals to the SMBus controller in adherence to the *System Management Bus (SMBus) Specification, Version 1.1*. These signals can be connected to other processors on the same SMBus.

The SM\_EP\_A[2:0] signals set the SMBus address for the memory device on the processor. These signals must be set at power up with a unique address per bus. They have an internal  $10\text{ k}\Omega \pm 5\%$  pull-down. To pull the SM\_EP\_A[2:0] signals to a logic high level, connect each signal to a  $100\text{ }\Omega \pm 5\%$  resistor tied to SM\_VCC. Refer to the section on SMBus Device Addressing in the Processor datasheet for addressing details.

The SM\_TS\_A[1:0] signals set the SMBus address for the thermal device on the processor. These signals must be set at power up with a unique address per bus. The SM\_TS\_A[1:0] can be set to logic high, logic low, or a high impedance state giving nine possible combinations of addresses. Refer to the section on SMBus Device Addressing in the Processor datasheet for addressing details. The SM\_TS\_A[1:0] signals do not have an internal pull-down and thus must be pulled to VSS or SM\_VCC with a  $1\text{ k}\Omega \pm 5\%$  or smaller resistor. Leaving the pins floating achieves a high-Z state.

The SM\_WP signal is a write protect signal for the memory device. Pulling this signal to SM\_VCC with a  $100\text{ }\Omega \pm 5\%$  resistor enables write protection. SM\_WP has an internal  $10\text{ k}\Omega$  pull-down.

### 5.3.5 System Bus COMP Routing Guidelines

Terminate the processor COMP[1:0] pins to ground through  $50\text{ }\Omega \pm 1\%$  resistors. Do not wire the COMP pins together—connect each pin to its own termination resistor.

Terminate the MCH HXRCOMP and HYRCOMP with a  $25\text{ }\Omega \pm 1\%$  resistor pull-down to ground. Terminate the MCH HXSWING and HYSWING using a  $150\text{ }\Omega \pm 1\%$  resistor pull-down to ground, and a  $301\text{ }\Omega \pm 1\%$  pull-up to VCC\_CPU, respectively. Use two  $0.01\text{ }\mu\text{F}$  decoupling capacitors.

### 5.3.6 BR[3:0]# Routing Guidelines

Connect BR[3:0]# as shown in Figure 5-10. The total bus length must be less than 20.2". BR3# and BR2# are not used and are pulled to VCC\_CPU.

Figure 5-10. BR[3:0]# Connection for DP Configuration

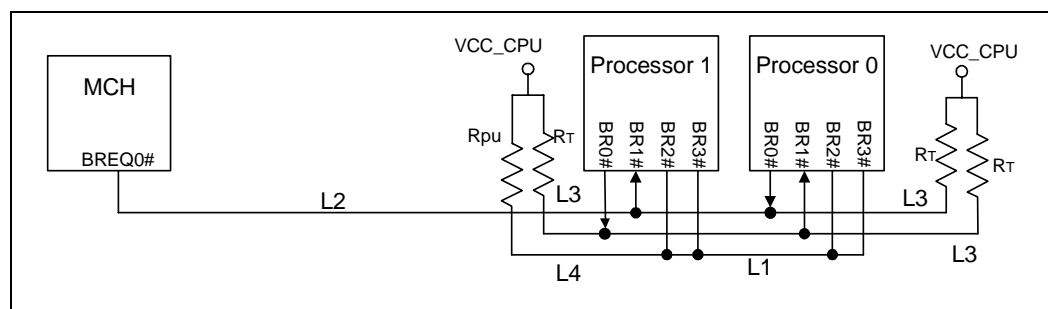


Table 5-7. BR[3:0]# Connection

Trace Impedance	L1 Processor-to-Processor	L2 Processor1 BR1# to Intel® MCH	L3 Processor-to-RT Stub	L4 Processor-to-R <sub>PU</sub> Stub	R <sub>T</sub>	R <sub>PU</sub>
50 $\Omega$	3.0 – 10.0"	15.7" max	1" max	3" max	$50\text{ }\Omega \pm 5\%$	$50\text{ }\Omega \pm 5\%$

### 5.3.7 OD TEN Signal Routing Guidelines

Processor 0, the end processor in a dual processor system, must have its on-die termination enabled. The termination value must be within 20% of the signal impedance ( $50\text{ }\Omega \pm 20\%$ ). To enable the on-die termination, pull the OD TEN pin to a high state by terminating it to VCC\_CPU through a  $50\text{ }\Omega \pm 20\%$  resistor. Processor 1, the middle agent, must have its on-die termination disabled. To disable on-die termination, pull the OD TEN pin to a low state by terminating it to ground through a  $50\text{ }\Omega \pm 20\%$  resistor.



### 5.3.8 TESTHI[6:0] Routing Guidelines

All TESTHI[6:0] pins must be connected to VCC\_CPU via pull-up resistors with a termination value within 20% of the signal impedance ( $50\ \Omega \pm 20\%$ ). TESTHI[3:0] may all be tied together and pulled up to VCC\_CPU with a single,  $50\ \Omega \pm 20\%$  resistor if desired. TESTHI[6:5] may also be tied together and pulled up to VCC\_CPU with a single  $50\ \Omega \pm 20\%$  resistor. However, boundary scan testing will not be functional if any TESTHI pins are pulled up together. TESTHI4 must always be pulled up independently from the other TESTHI pins regardless of the usage of boundary scan.

### 5.3.9 SKTOCC# Signal Routing Guidelines

The SKTOCC# signal is an output from the processor used as an indication of whether a processor is installed or not. It is asserted low when a processor is installed in the socket, and floats when no processor is present. If this signal is used on the board, the designer can use a pull-up to prevent floating. SKTOCC# can be used to disable the VRM or VRD output for unpopulated processor sockets or the power supply output when no processors are installed and other features.

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# Memory Interface Routing Guidelines 6

The MCH memory interface consists of two DDR memory channels that operate in “lock-step.” Each channel consists of 64 data and 8 ECC bits. Logically, this is one 144-bit wide memory bus; electrically, each channel is separate.

This section covers routing guidelines for the DDR interfaces. Note that these guidelines apply to both channel A and channel B. Each DDR interface has seven signal types: Source Synchronous Signals, Command Clocks, Source Clocked Signals, Chip Selects, Clock Enable, Receive Enable, and Miscellaneous. [Table 6-1](#) summarizes the signal groupings. The MCH contains two complete sets of these signals, one set per channel. Refer to the *Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet* for details on the signals listed in [Table 6-1](#).

**Table 6-1. DDR Channel Signal Groups**

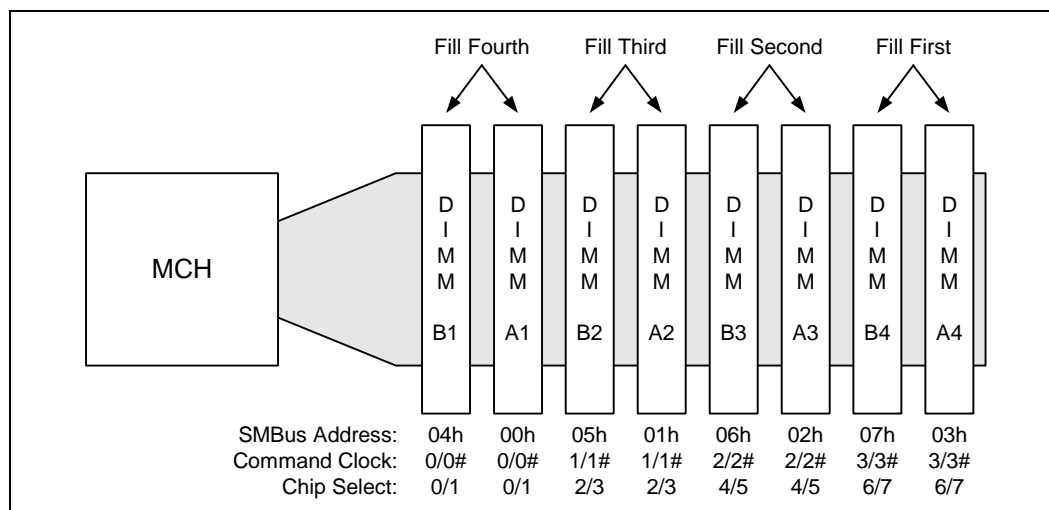
Group	Signal
Source Synchronous Signals	DQS[17:0] DQ[63:0] CB[7:0]
Command Clocks	CMDCLK[3:0] CMDCLK[3:0]#
Source Clocked Signals	MA[12:0] RAS# CAS# WE# BA[1:0]
Chip Selects	CS#[7:0]
Clock Enable	CKE
Receive Enable	RCVENIN# RCVENOUT#
Miscellaneous	DDRCOMP DDRCVOH DDRCVOL DDRVREF[5:0]

## 6.1 DDR Overview

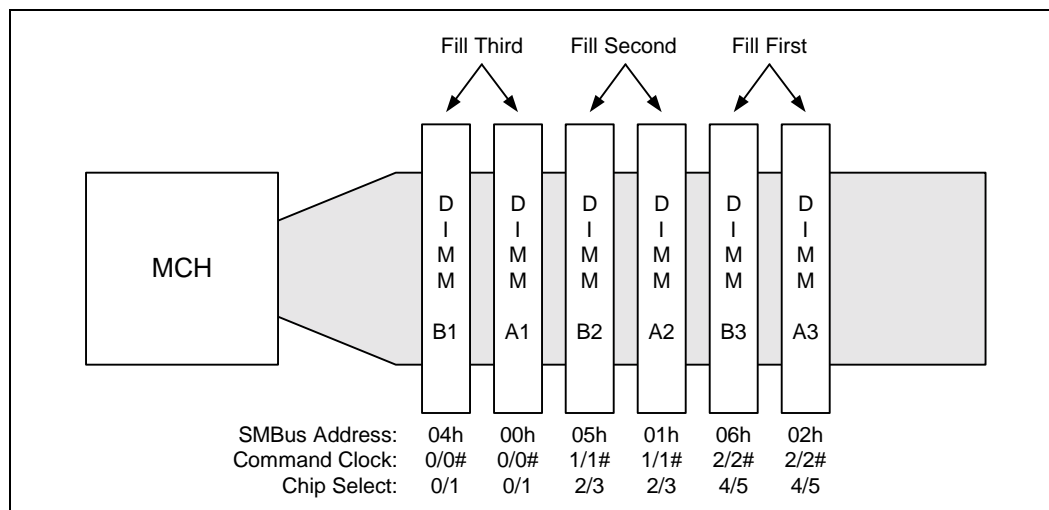
Figure 6-2 and Figure 6-1 show both channels being routed to a single “bank” of eight DIMMs. The DIMMs are physically interleaved. Intel recommends using this ordering, starting with Channel B closest to the MCH, for optimal routing.

The platform requires DDR DIMMs to be populated in-order, starting with the 2 DIMMs furthest from the MCH in a “fill-farthest” approach (see Figure 6-2 and Figure 6-1). This recommendation is based on the signal integrity requirements of the DDR interface. Intel’s recommendation is to conduct this check for correct DIMM placement during BIOS initialization. Additionally, it is strongly recommended that all designs follow the DIMM ordering, SMBus Addressing, Command Clock routing and Chip Select routing documented in Figure 6-2 and Figure 6-1. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel. Designs with fewer than 3 DIMMs should follow the pattern shown in Figure 6-2 and Figure 6-1.

**Figure 6-1. 4 DIMM per Channel Implementation**

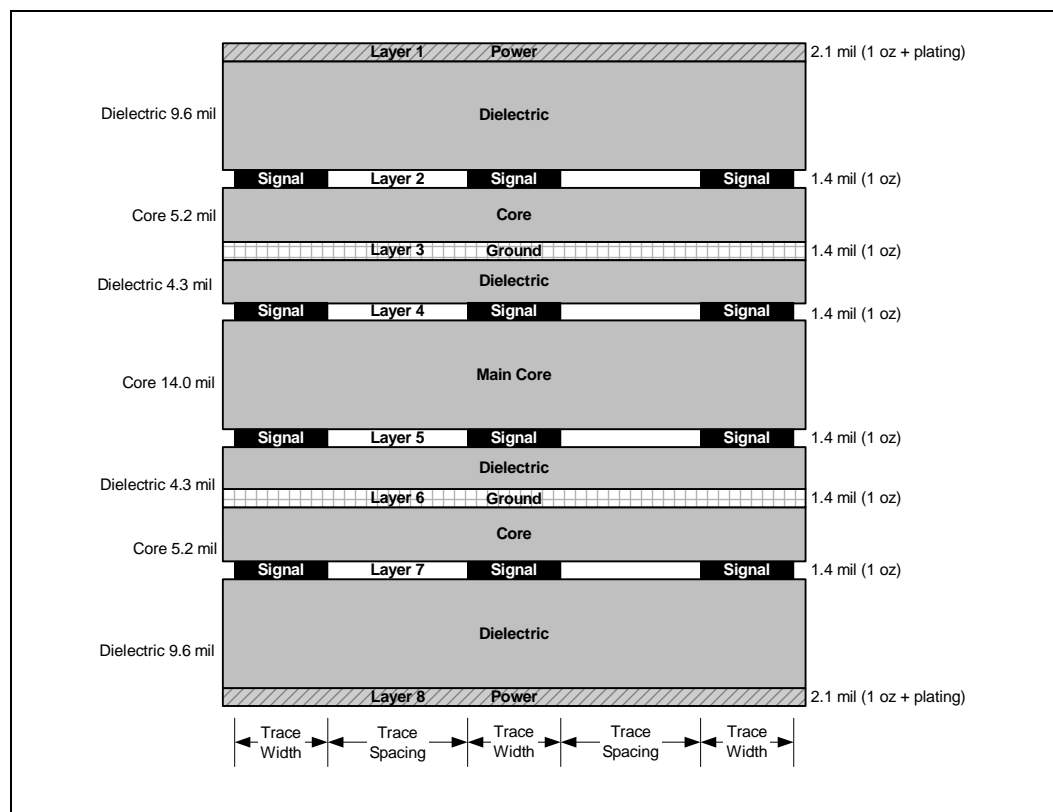


**Figure 6-2. 3 DIMM per Channel Implementation**



The DDR interface requires a nominal impedance ( $Z_0$ ) of  $50\ \Omega \pm 10\%$ . Using the recommended stackup, all routing layers yield  $50\ \Omega$  nominal impedance when using 5 mil wide traces. Route all DDR signals 5/15 (5 mils wide with 15 mil spacing) as shown in Figure 6-3 with the exception of CKE, CMDCLK[3:0], and CMDCLK[3:0]#. For CMDCLK routing rules, refer to Section 6.3 and Figure 6-8. For CKE routing rules, refer to Section 6.6 and Figure 6-3. Route layers 4 and 5 orthogonal to each other to minimize crosstalk.

**Figure 6-3. Trace Width and Spacing for All DDR Signals Except CMDCLK/CMDCLK#**



**NOTES:**

1. Traces on layers 4 and 5 must be routed orthogonally to each other to minimize the effects of crosstalk.
2. Source Synch., Source Clocked, and CS# are routed 5/15.
3. CKE is routed 7.5/15.

## 6.2 Source Synchronous Signal Group

The MCH source synchronous signals are divided into groups consisting of data bits (DQ) and check bits (CB). An associated strobe (DQS) exists for each DQ and CB group, as shown in [Table 6-2](#). The MCH supports both x4 and x8 devices, and the number of signals in each data group depends on the type of devices that are populated. For example, if x4 devices are populated, the 72-bit channel is divided into 18 data groups (16 groups consisting of 4 data bits each, and 2 groups consisting of 4 check bits each). One DQS is associated with each of these groups (18 total). Likewise, if x8 devices are populated, the 72-bit channel is divided into a total of nine data groups. In this case, only 9 of the 18 strobes are used.

**Table 6-2. DQ/CB to DQS Mapping**

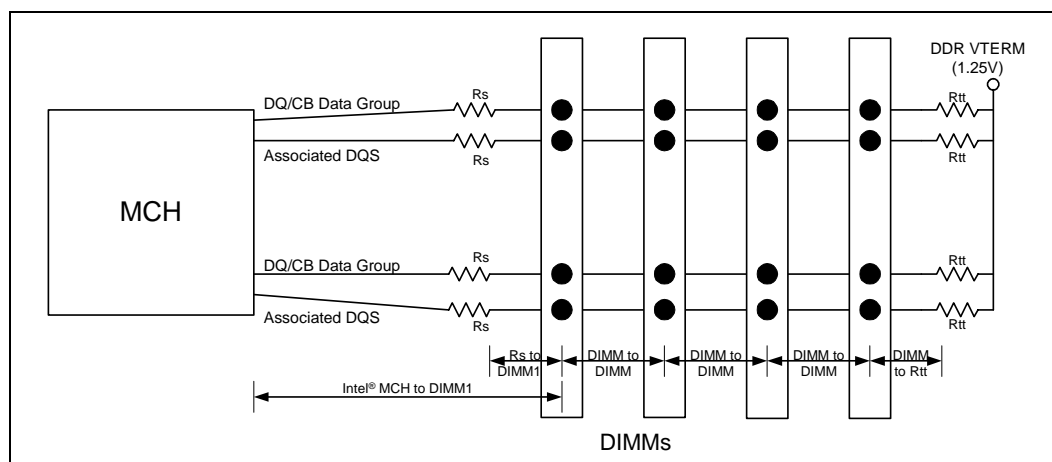
Data Group	Associated Strobe <sup>1</sup>
DQ[7:0]	DQS0, DQS9
DQ[15:8]	DQS1, DQS10
DQ[23:16]	DQS2, DQS11
DQ[31:24]	DQS3, DQS12
DQ[39:32]	DQS4, DQS13
DQ[47:40]	DQS5, DQS14
DQ[55:48]	DQS6, DQS15
DQ[63:56]	DQS7, DQS16
CB[7:0]	DQS8, DQS17

**NOTE:** <sup>1</sup>In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

[Figure 6-4](#) shows the trace length requirements for the DQ, DQS and CB signals. All signals in a data group must be length matched to the associated DQs within  $\pm 100$  mils, as shown in [Figure 6-5](#). In addition, each DQS at a particular DIMM must be length matched to the CMDCLK/CMDCLK# pair that is routed to that particular DIMM within  $\pm 1.75$ ", as shown in [Figure 6-6](#). Length matching past the last DIMM connector is not critical. Route all data signals and their associated strobes on the same layer. Layer changes are only recommended at MCH ball breakout and at the series resistor. The source synchronous signals require  $10\ \Omega \pm 2\%$  series termination resistors placed close to and before the first DIMM connector, and  $22\ \Omega \pm 2\%$  parallel termination resistors placed as close as possible and after the last DIMM connector (within 0.8").

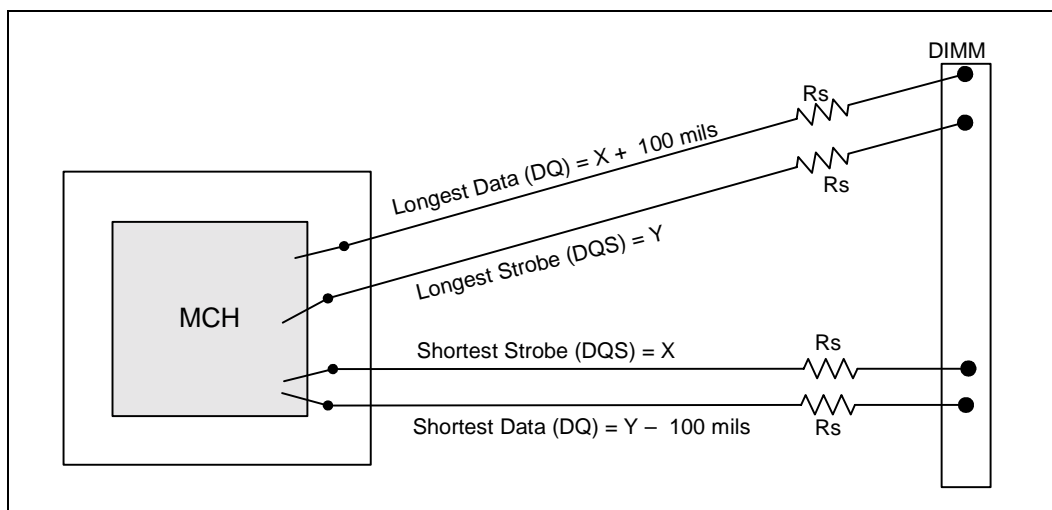
**Table 6-3. Source Synchronous Signal Group Routing Guidelines**

Parameter	Intel® E7500	Reference
Signal Group	DQ[63:0], CB[7:0], DQS[17:0]	
Topology	Daisy Chain	Figure 6-4
Reference Plane	Ground	Figure 6-3
MCH to Rtt (Zo)	$50\ \Omega \pm 10\%$	Figure 6-3
MCH to Rtt Trace Width	5 mil	Figure 6-3
Nominal Trace Spacing	15 mil	Figure 6-3
Trace Length – MCH to DIMM1	1.8" to 6.0"	Figure 6-4
Trace Length – Rs to DIMM1	< 0.8"	Figure 6-4
Trace Length – DIMM to DIMM	0.8" to 1.2"	Figure 6-4
Trace Length – DIMM to Rtt	< 0.8"	Figure 6-4
Series Resistor (Rs)	$10\ \Omega \pm 2\%$	Figure 6-4
Termination Resistor (Rtt)	$22\ \Omega \pm 2\%$	Figure 6-4
MCH Breakout Guidelines	5/5, < 500 mil	
Length Tuning Requirements	DQ to DQS: $\pm 100$ mil DQS to CMDCLK pair: $\pm 1750$ mil	Figure 6-5 Figure 6-6

**Figure 6-4. Source Synchronous Topology**

**NOTES:**

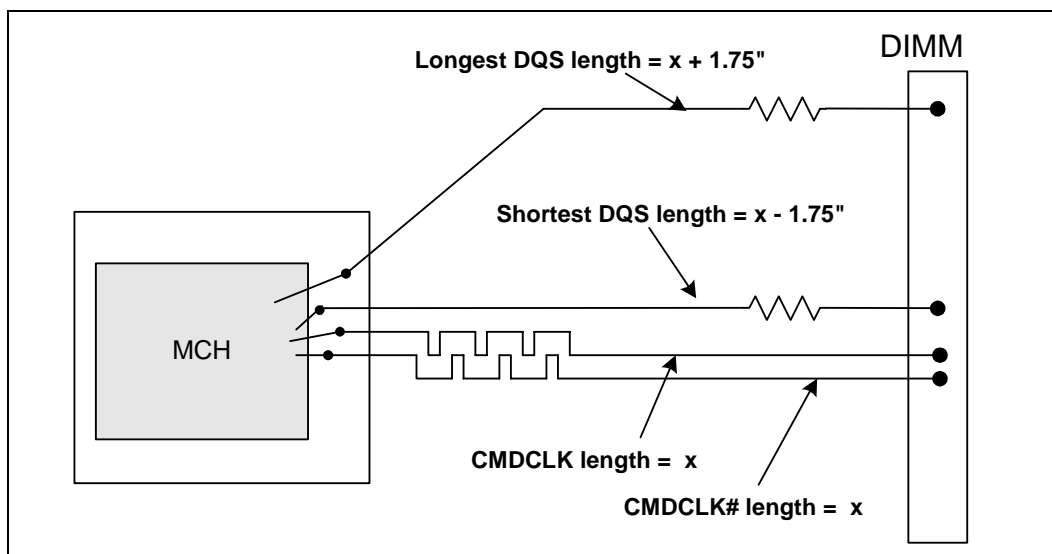
1. Indicated lengths measure from the MCH pin to the DIMM connector pin (including the series resistor).

Figure 6-5. Trace Length Matching Requirements for Source Synchronous Routing

**NOTES:**

1. The DIMM displayed represents **any** DIMM. All DIMMs must be length matched within the specified distance. A simple method to do this is to length match the MCH to the first DIMM within the specified tolerance and then match all the signals DIMM to DIMM.
2. There are 8 Data lines (DQ) per group. For simplicity purposes, only the longest and the shortest are represented here.
3. Indicated lengths measure from the MCH die pad to the DIMM connector pin (including the series resistor).

Figure 6-6. DQS To CMDCLK Pair Length Matching

**NOTES:**

1. Indicated lengths measure from the MCH die pad to the DIMM connector pin (including the series resistor).



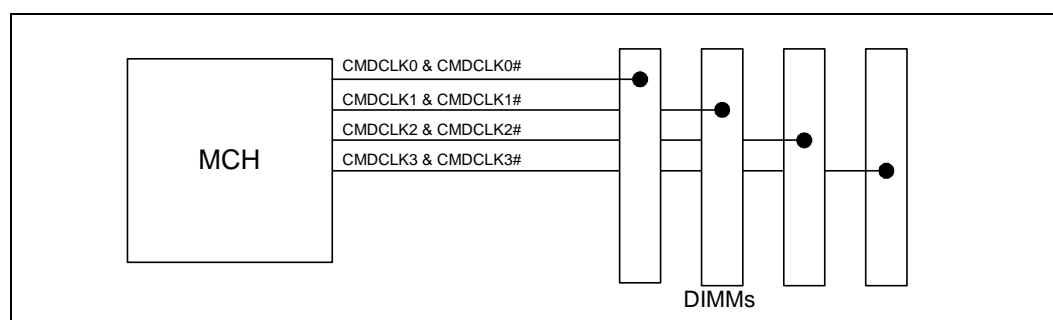
## 6.3 Command Clock Routing

Only one differential clock pair is routed to each DIMM connector because the MCH only supports registered DDR DIMMs. All CMDCLK/CMDCLK# termination is on the DIMM modules. Route each clock and its complement adjacent to each other. The two complimentary signals (e.g., CMDCLK0 and CMDCLK0#) must be length matched to each other within  $\pm 2$  mils. Excluding breakout, the maximum recommended layer changes is one. Ensure that the reference plane does not change when switching layer.

**Table 6-4. Command Clock Pair Routing Guidelines**

Parameter	Intel® E7500	Reference
Signal Group	CMDCLK[3:0], CMDCLK[3:0]#	
Topology	Point to point	Figure 6-7
Reference Plane	Ground	Figure 6-8
Differential Trace Impedance ( $Z_0$ )	100 $\Omega \pm 10\%$	Figure 6-8
Nominal Trace Width	5 mil	Figure 6-8
Trace Spacing to Complement	5 mil	Figure 6-8
Trace Spacing to Other Traces	20 mil	Figure 6-8
Trace Length – MCH to DIMM1	2.1" to 10.0"	Figure 6-7
Trace Length – MCH to DIMM2	2.1" to 10.0"	Figure 6-7
Trace Length – MCH to DIMM3	2.1" to 10.0"	Figure 6-7
Trace Length – MCH to DIMM4	2.1" to 10.0"	Figure 6-7
MCH Breakout Guidelines	5/5, < 500 mil	
Length Tuning Requirements	CMDCLK to CMDCLK#: $\pm 2$ mil CMDCLK pair to pair: within $\pm 4.0$ in. CMDCLK pair to DQS pair: $\pm 1.75$ in. CMDCLK pair to Source Clocked Signal: $\pm 2.0$ in.	Figure 6-7 Figure 6-6 Figure 6-9

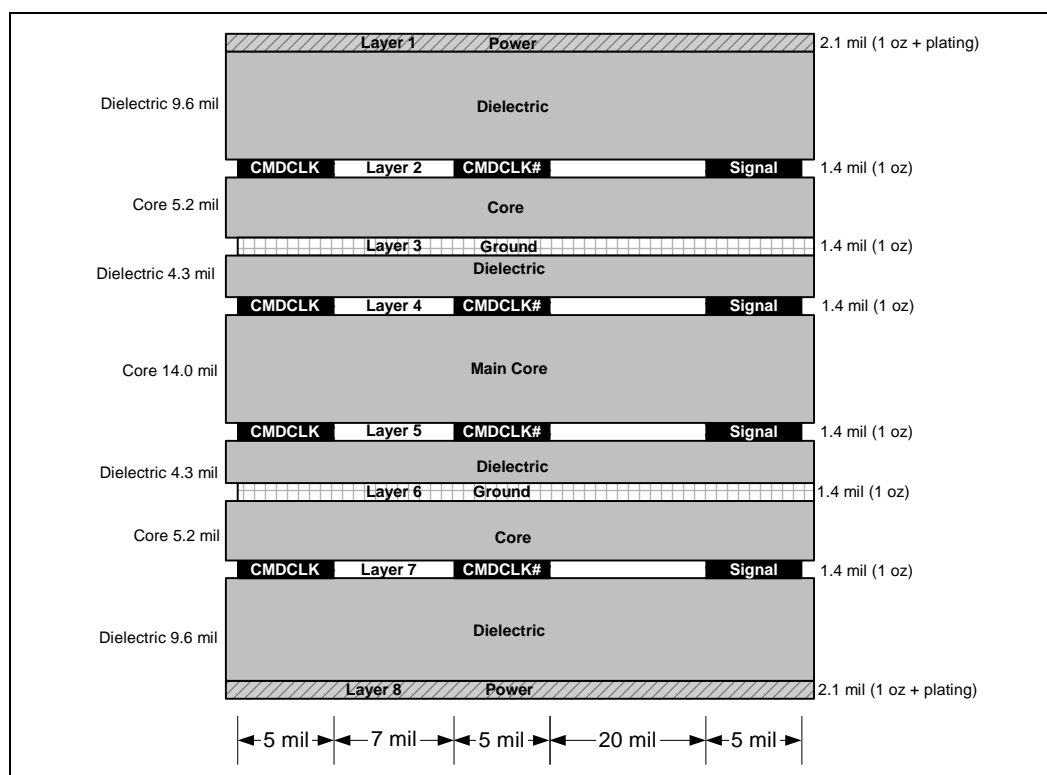
**Figure 6-7. Command Clock Topology**



**NOTES:**

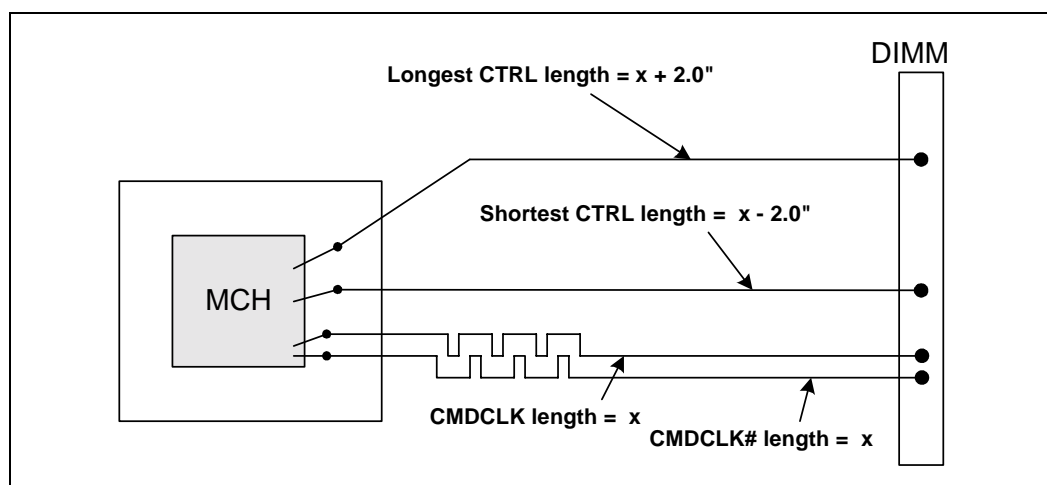
1. CMDCLK/CMDCLK# must be matched to within  $\pm 2$  mils using package trace length compensation.
2. The total trace length difference of any two CMDCLK/CMDCLK# pairs cannot exceed 4 inches for timing reasons.
3. For 3-DIMM solutions, treat the CMDCLK3/CMDCLK3# pair as a no connect.
4. Indicated lengths measure from the MCH pin to the DIMM connector pin.

Figure 6-8. Trace Width/Spacing for CMDCLK/CMDCLK# Routing



**NOTE:** The Intel E7500 MCH may also use a 5 mil space between CMDCLK complements.

Figure 6-9. Length Matching Requirements for Source Clocked Signal, CKE, and CS[7:0]#



**NOTES:**

1. Indicated lengths measure from the MCH die pad to the DIMM connector pin.

## 6.4 Source Clocked Signal Group Routing

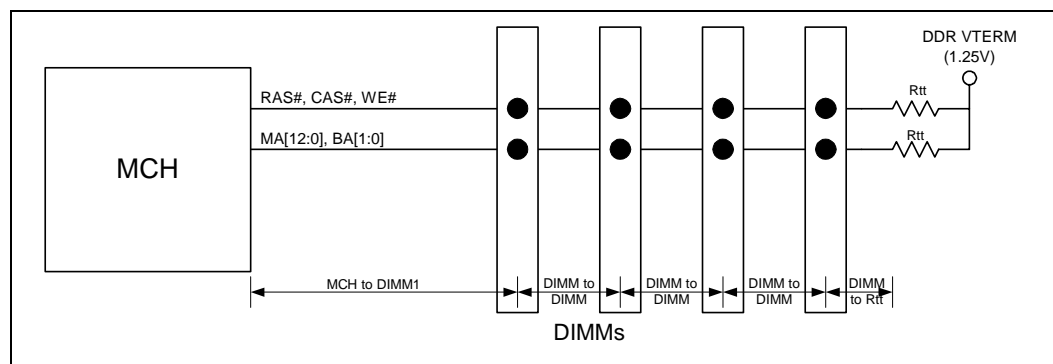
The MCH drives the command clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The source-clocked signals are “clocked” into the DIMMs using the command clock signals. Because the MCH drives the command clock signals and the source-clocked signals together, these signals can be source clocked. That is, the MCH drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. Therefore, the critical timing is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

The source-clocked signals have a topology similar to the source synchronous signals. These signals require parallel termination resistors ( $R_{tt}$ ) to DDR VTERM. The MCH requires matching the lengths of the source-clocked signals to the lengths of the command clocks for each DIMM within 2.0 inches. For example, if CMDCLK0 and CMDCLK0# are 3 inches long, all source clocked signals from MCH to the DIMM that CMDCLK0/CMDCLK0# is routed to should be 3 inches  $\pm$  2.0 inches.

**Table 6-5. Source Clocked Signal Group Routing Guidelines**

Parameter	Intel® E7500	Reference
Signal Group	RAS#, CAS#, WE#, MA[12:0], BA[1:0]	
Topology	Daisy Chain	Figure 6-10
Reference Plane	Ground	Figure 6-3
Trace Impedance ( $Z_0$ )	50 $\Omega \pm 10\%$	Figure 6-3
Nominal Trace Width	5 mil	Figure 6-3
Nominal Trace Spacing	15 mil	Figure 6-3
Trace Length – MCH to DIMM1	1.8” to 6.0”	Figure 6-10
Trace Length – DIMM to DIMM	0.8” to 1.2”	Figure 6-10
Trace Length – DIMM to $R_{tt}$	< 0.8”	Figure 6-10
Termination Resistor ( $R_{tt}$ )	22 $\Omega \pm 2\%$	Figure 6-10
MCH Breakout Guidelines	5/5, < 500 mil	
Length Tuning Requirements	To CMDCLK pair: $\pm 2.0$ ”	Figure 6-9

**Figure 6-10. Source Clocked Signal Topology**



**NOTE:** Indicated lengths measure from the MCH pin to the DIMM connector pin.

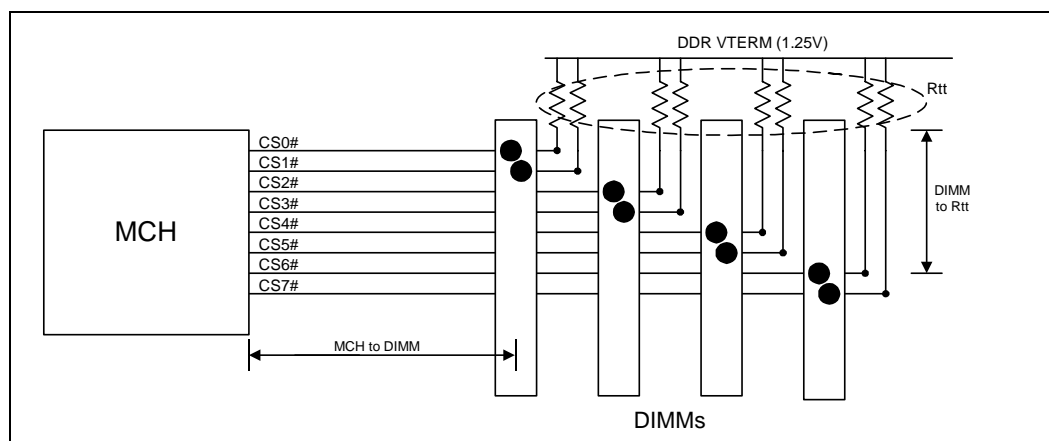
## 6.5 Chip Select Routing

The MCH provides eight chip select signals. Two chip selects must be routed to each DIMM (one for each side). The E7500 chip selects for each DIMM must be length matched to the corresponding clock within  $\pm 2.0$  inches and require parallel termination resistors ( $R_{tt}$ ) to DDR VTERM, placed within 3 inches of their associated connector.

**Table 6-6. Chip Select Routing Guidelines**

Parameter	Intel® E7500	Reference
Signal Group	CS[7:0]#	
Topology	Point to Point	Figure 6-11
Reference Plane	Ground	Figure 6-3
Trace Impedance ( $Z_0$ )	$50 \Omega \pm 10\%$	Figure 6-3
Nominal Trace Width	5 mil	Figure 6-3
Nominal Trace Spacing	15 mil	Figure 6-3
Trace Length – MCH to DIMM1	1.8" to 9.6"	Figure 6-11
Trace Length – MCH to DIMM2	1.8" to 9.6"	Figure 6-11
Trace Length – MCH to DIMM3	1.8" to 9.6"	Figure 6-11
Trace Length – MCH to DIMM4	1.8" to 9.6"	Figure 6-11
Trace Length – DIMM to $R_{tt}$	< 3.0"	Figure 6-11
Termination Resistor ( $R_{tt}$ )	$22 \Omega \pm 2\%$	Figure 6-11
MCH Breakout Guidelines	5/5, < 500 mil	
Length Tuning Requirements	To CMDCLK pair: $\pm 2.0$ "	Figure 6-9

**Figure 6-11. Chip Select Topology**



**NOTES:**

1. For 3-DIMM solutions, treat CS6# and CS7# as a no connect.
2. Indicated lengths measure from the MCH pin to the DIMM connector pin, and from the DIMM connector to the parallel termination resistor pin.

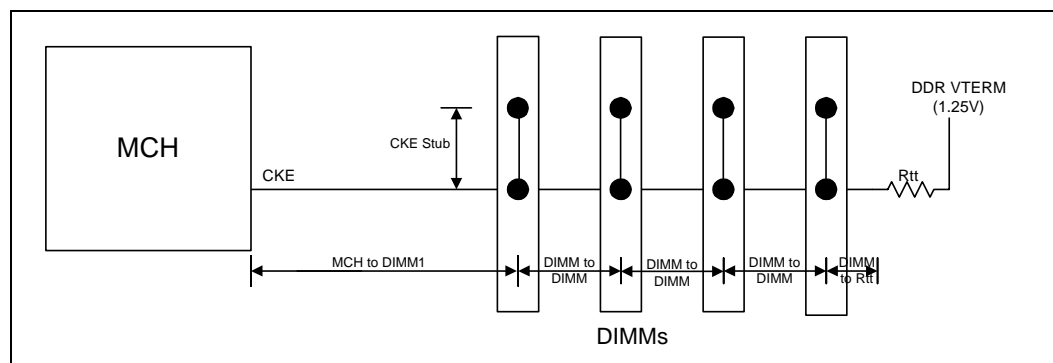
## 6.6 Clock Enable Routing

The MCH provides a single clock enable (CKE) signal. This signal is used during initialization to indicate that valid power and clocks are being applied to the DIMMs. Because the CKE signal has higher loading, it requires a lower impedance. The recommended impedance for the CKE signal is  $40\ \Omega$ . This can be achieved using a 7.5 mil wide trace on the recommended stackup (refer to [Figure 6-3](#)). It is acceptable to route the CKE signal 5 mils wide when breaking out of the MCH. The CKE signal requires a parallel termination resistor ( $R_{tt}$ ) to DDR VTERM placed as close to the last DIMM connector as possible.

**Table 6-7. Clock Enable Routing Guidelines**

Parameter	Intel® E7500	Reference
Signal Group	CKE	
Topology	Daisy Chain with Stubs	<a href="#">Figure 6-12</a>
Reference Plane	Ground	<a href="#">Figure 6-3</a>
Trace Impedance ( $Z_0$ )	$40\ \Omega \pm 10\%$	<a href="#">Figure 6-3</a>
Nominal Trace Width	7.5 mil	<a href="#">Figure 6-3</a>
Nominal Trace Spacing	15 mil	<a href="#">Figure 6-3</a>
Trace Length – MCH to DIMM1	1.8" to 6.0"	<a href="#">Figure 6-12</a>
Trace Length – DIMM to DIMM	0.8" to 1.2"	<a href="#">Figure 6-12</a>
Trace Length – CKE Stub	< 300 mil	<a href="#">Figure 6-12</a>
Trace Length – DIMM to $R_{tt}$	< 0.8"	<a href="#">Figure 6-12</a>
Termination Resistor ( $R_{tt}$ )	$22\ \Omega \pm 2\%$	<a href="#">Figure 6-12</a>
MCH Breakout Guidelines	5/5, < 500 mil	
Length Tuning Requirements	To CMDCLK pair: $\pm 2.0$ "	<a href="#">Figure 6-9</a>

**Figure 6-12. CKE Topology**

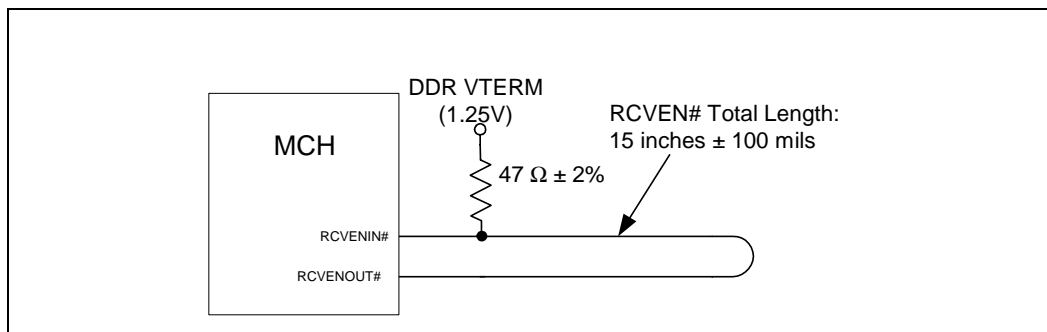


**NOTE:** Indicated lengths measure from the MCH pin to the DIMM connector pin.

## 6.7 Enable Signal (RCVEN#)

The MCH uses the “receive enable” (RCVEN#) signal to determine the approximate DIMM round-trip flight time (command flight + data flight). Two pins exist on the MCH to facilitate the use of RCVEN#: RCVENOUT# and RCVENIN#. RCVENOUT# is an output of the MCH, and RCVENIN# is an input to the MCH. The board designer must connect RCVENOUT# to RCVENIN#. The length of the RCVEN# signal trace must be  $15'' \pm 100$  mils. [Figure 6-13](#) illustrates the routing recommendations of the RCVEN# signal.

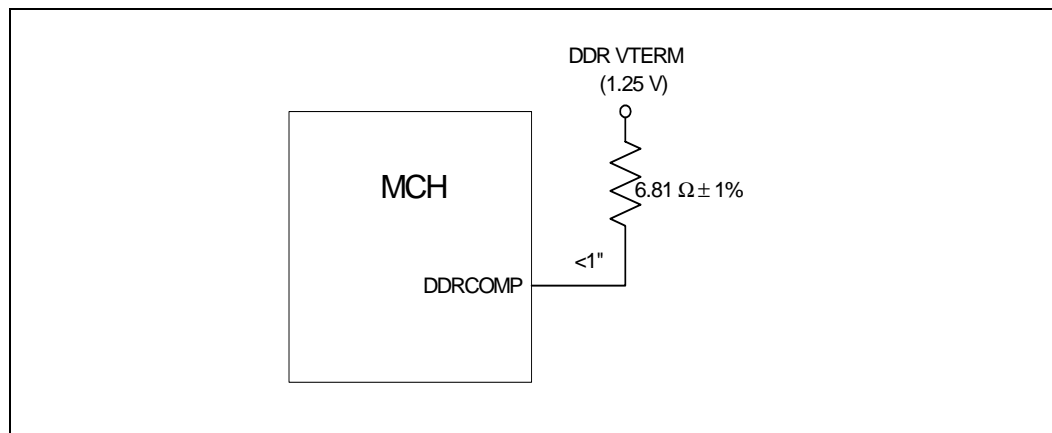
**Figure 6-13. Receive Enable Signal Routing Guidelines**



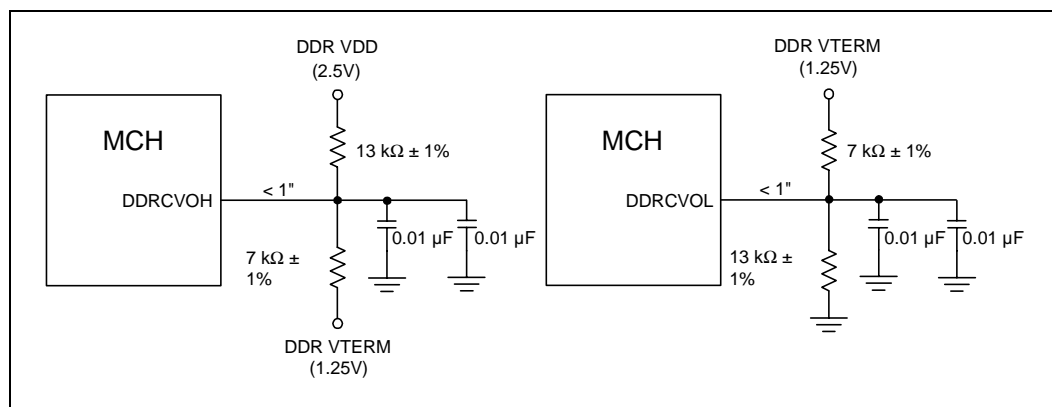
## 6.8 Miscellaneous Signals

The MCH uses a compensation signal to adjust buffer characteristics and output voltage swing over temperature, process, and voltage skew. Calibration is done periodically by sampling the DDRCOMP, DDRCVOH, and DDRCVOL pins on the MCH. Connect DDRCOMP to the DDR termination voltage (1.25 V) through a  $6.81\ \Omega \pm 1\%$  resistor as illustrated in Figure 6-14, and place the resistor within 1 in. of the MCH. Likewise, keep the voltage divider networks within 1 in. of the MCH (see Figure 6-15).

**Figure 6-14. DDRCOMP Resistive Compensation**



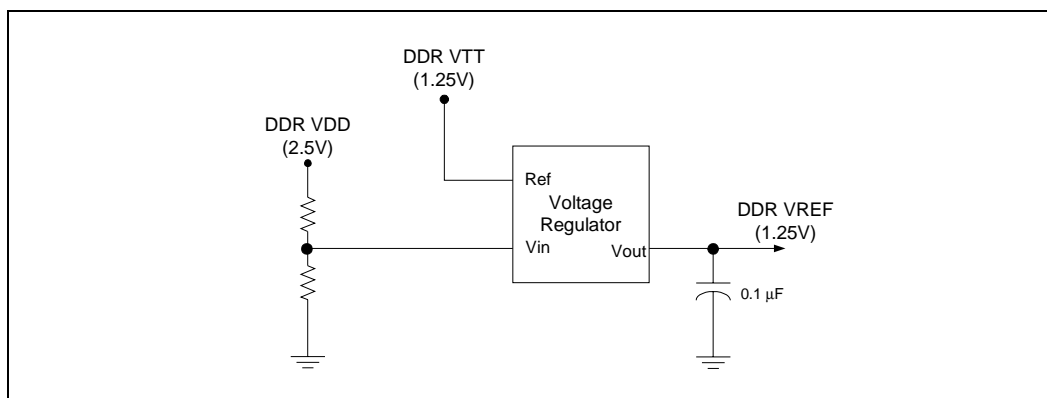
**Figure 6-15. DDRCVOL and DDRCVOH Resistive Compensation**



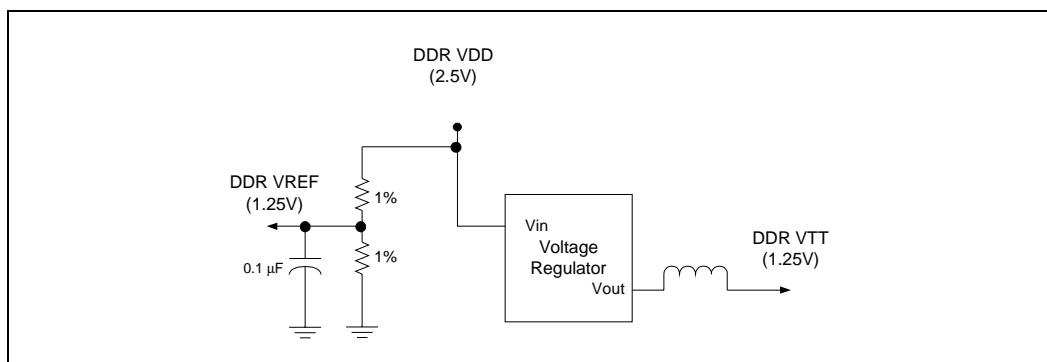
## 6.9 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DRAM devices and the MCH to determine the logic level being driven on the data, strobe, and control signals. VREF of the receiving device must track changes in VTT to maximize DDR interface margin. If a voltage regulator is used, it must reference VTT (See [Figure 6-16](#)). If a local resistor divider is used, VREF and VTT must have a common source voltage between them (i.e., both VREF and VTT are derived from the same voltage plane), and 1% resistors should be used (See [Figure 6-17](#)). Decouple VREF locally at the divider and DIMMs/MCH using one 0.1µF capacitor per VREF pin.

**Figure 6-16. DDR VREF Voltage Regulator**



**Figure 6-17. DDR VREF Voltage Divider**

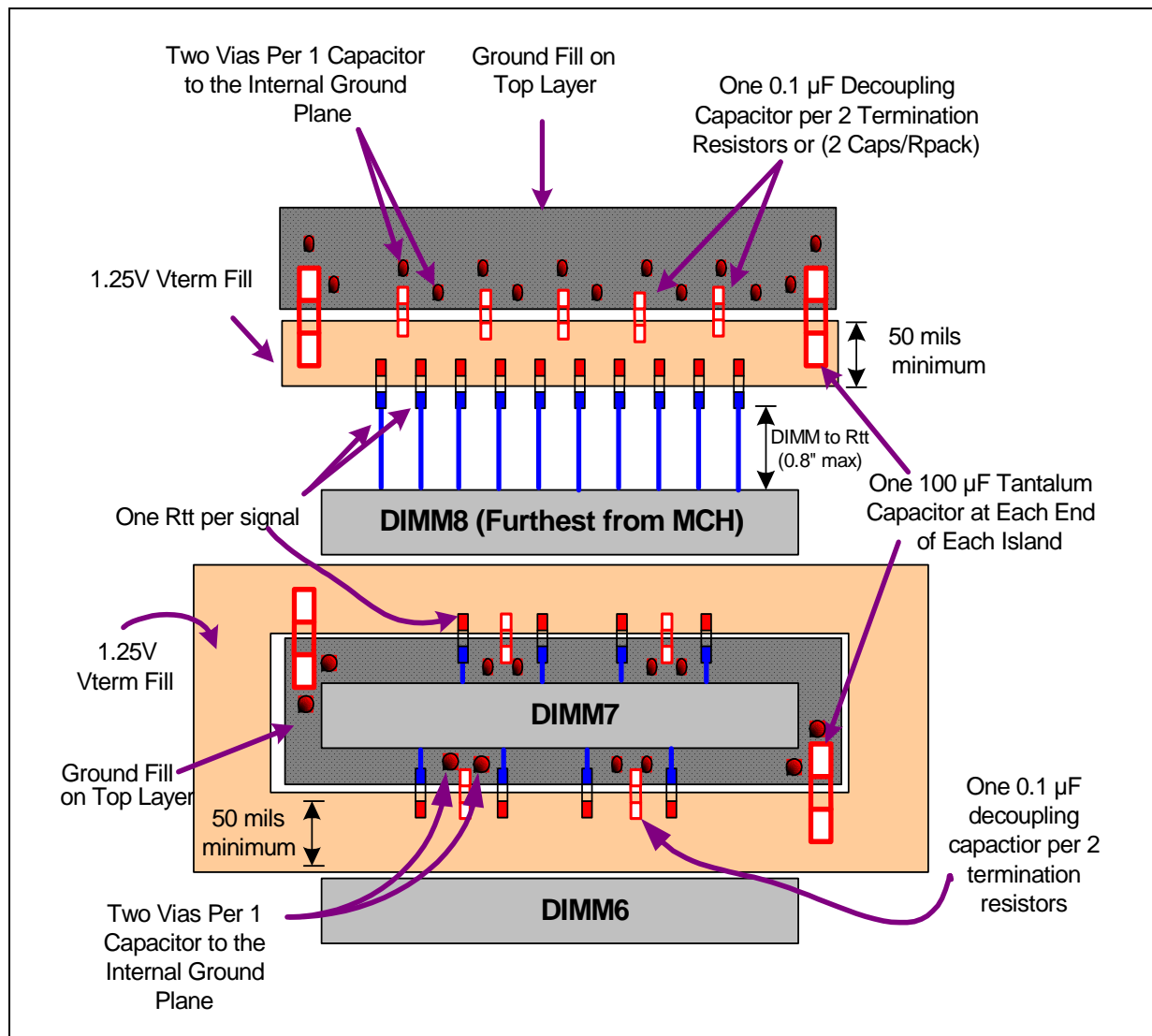




## 6.10 DDR Signal Termination

Place a 1.25 V termination plane on the top layer just beyond the DIMM connector furthest from the MCH on each channel, as shown in Figure 6-18. The VTERM island must be at least 50 mils wide. Use this termination plane to terminate all DIMM signals, using one  $22\ \Omega \pm 2\%$  resistor per signal. Decouple the VTERM plane using one  $0.1\ \mu\text{F}$  decoupling capacitor per two termination resistors. In addition, place one  $100\ \mu\text{F}$  Tantalum capacitor on each end of each termination island for bulk decoupling. Each decoupling capacitor must have at least 2 vias between the top layer ground fill, and the internal ground plane. Refer to Figure 6-18.

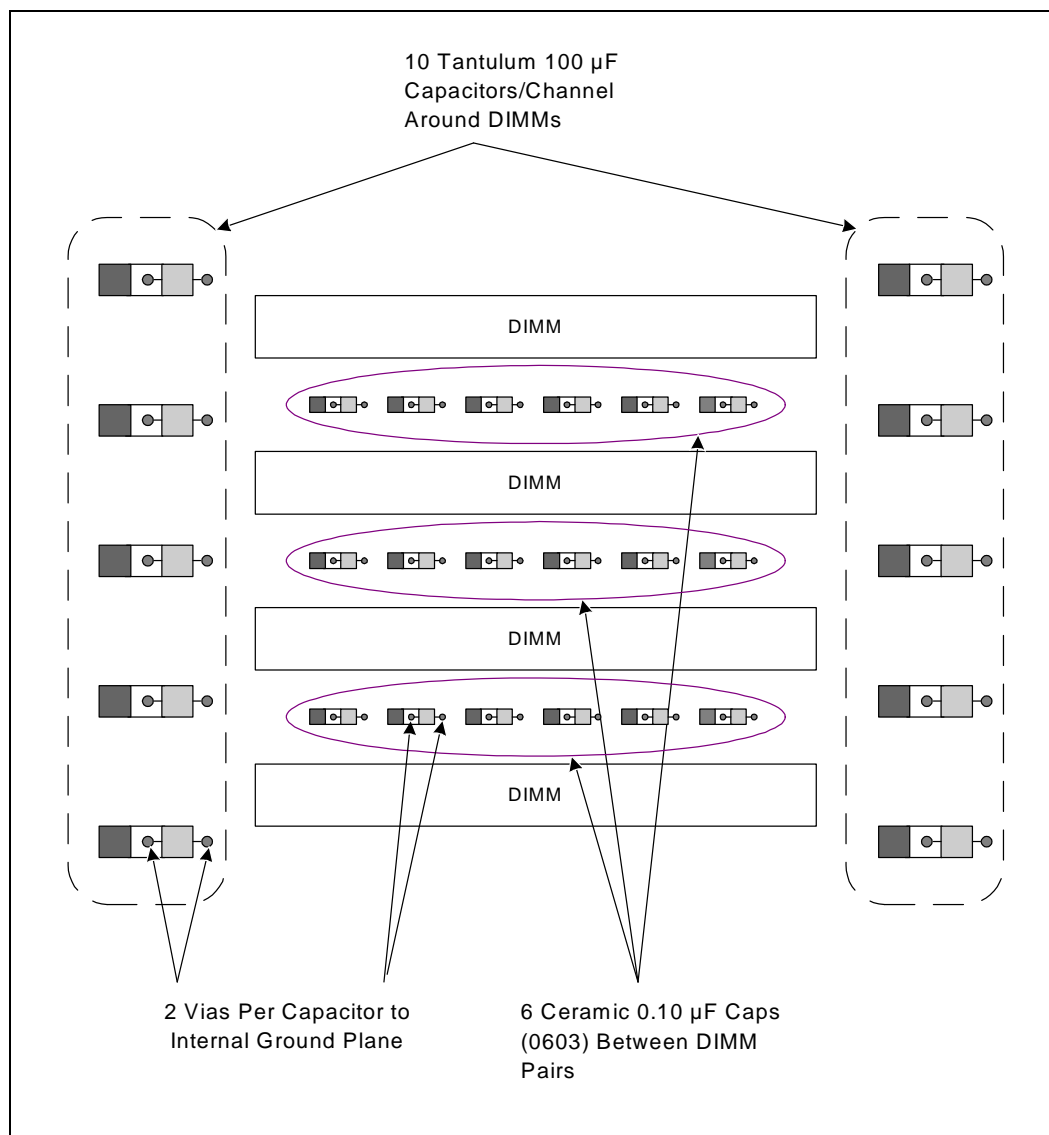
Figure 6-18. DDR VTerm Plane



## 6.11 Decoupling Requirements

Decouple the DIMM connectors as shown in Figure 6-19. Place six ceramic 0.1  $\mu\text{F}$  (0603) capacitors between adjacent DIMM connectors. Place ten Tantalum 100  $\mu\text{F}$  capacitors per channel around the DIMM connectors, keeping them within 0.5" of the edge of the DIMM connectors. Again, be sure to implement two vias per capacitor (ceramic and tantalum) to the internal ground plane.

Figure 6-19. DIMM Decoupling



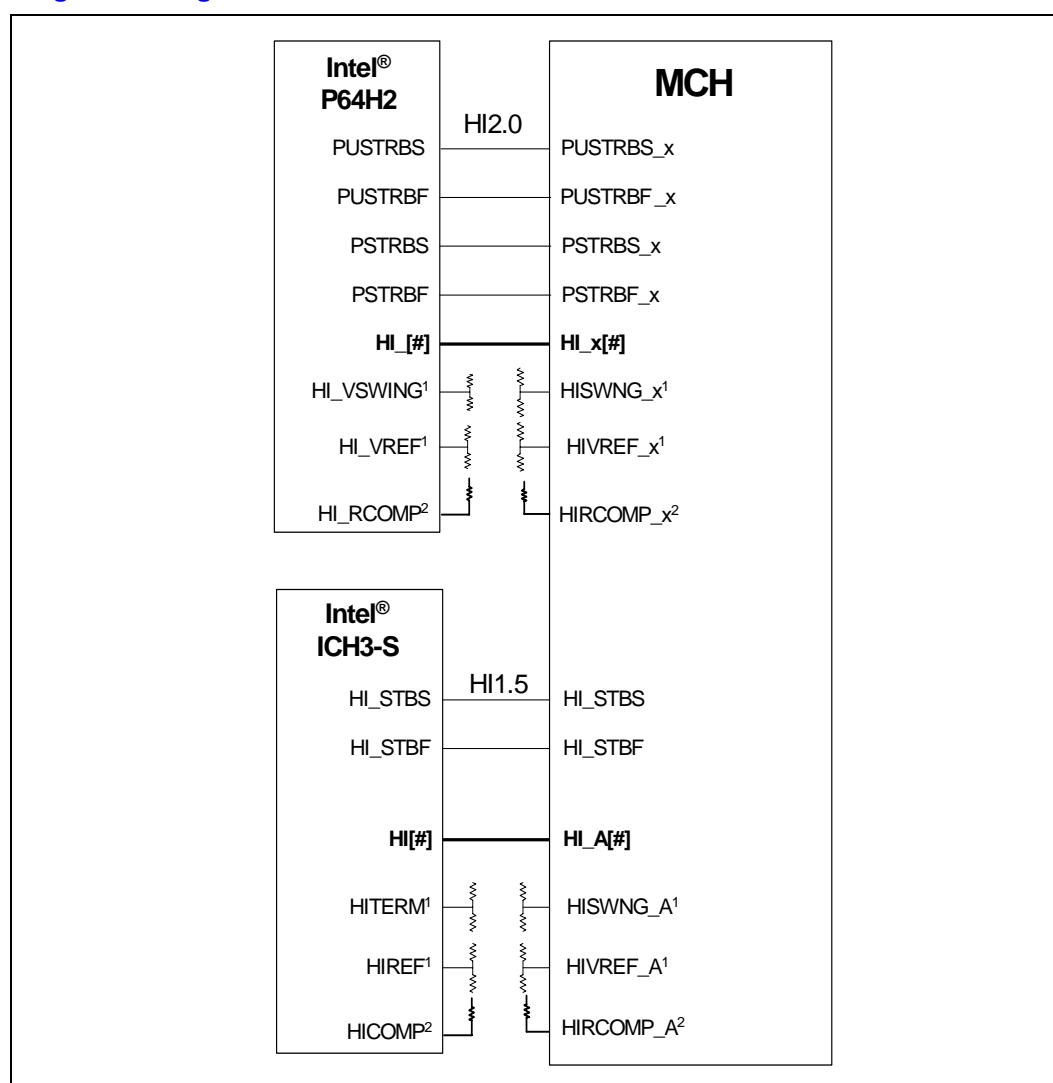
# Hub Interface

# 7

## 7.1 Signal Naming Convention

Figure 7-1 has the Hub Interface 2.0 and Hub Interface 1.5 signal naming convention for each component. This figure is intended to give a quick naming cross reference to designers. The specific guidelines and implementations on these signals are given in the following sections. Note that throughout the document, the 'x' part of the MCH signal has been dropped for simplicity.

**Figure 7-1. Signal Naming Convention on Both Sides of the Hub Interfaces**



**NOTES:**

1. These signals have individual resistor dividers. For specific values, refer to [Figure 7-5](#) and [Figure 7-8](#).
2. These signals have individual pull-up resistors. For specific values, refer to [Figure 7-6](#) and [Figure 7-9](#).
3. Signal names for HI2.0 on the MCH: x = B, C, or D.

## 7.2 Hub Interface 2.0 Implementation

The MCH, and P64H2 ballout assignments are optimized to simplify the hub interface routing between these devices. To allow for greater flexibility in design, a connector can be placed on the interface to access a HI2.0 agent that resides on an adapter card. The typical card implementation uses an extension to the 3.3 V PCI-64 connector that provides an additional 70 pins for HI2.0. Power, JTAG and SMBus signals are taken from the PCI portion of the connector. The remaining PCI signals are unused. This approach provides the flexibility to allow either a PCI/PCI-X card or a HI2.0 card, to be populated in the slot.

For the 16-bit Hub Interface, HI[7:0] and HI[20] are associated with PSTRBF and PSTRBS, and HI[15:8] and HI[21] are associated with PWSTRBF and PWSTRBS. HI[19:16] are common clock signals; they are sampled using CLK66. The three hub interfaces on the MCH are functionally and electrically identical. Therefore, these guidelines apply to all three hub interfaces.

**Table 7-1. Hub Interface 2.0 Signal/Strobe Association**

Data Group	Associated Strobes
HI[7:0] HI[20]	PSTRBF PSTRBS
HI[15:8] HI[21]	PWSTRBF PWSTRBS

### 7.2.1 Hub Interface 2.0 High-Speed Routing Guidelines

This section documents the routing guidelines for the Hub Interface 2.0. The Hub Interface 2.0 signal groups are listed in Table 7-2. The general routing guidelines for the Hub Interface 2.0 signals are given in Table 7-3.

**Table 7-2. Hub Interface 2.0 Signal Groups**

Group	Signal	
	MCH	Intel® P64H2
Common Clock Signals	HI[19:16]_x	HI[19:16]
Source Synchronous Signals	HI[21:20]_x, HI[15:0]_x, PSTRBF, PSTRBS, PWSTRBF, PWSTRBS	HI[21:20], HI[15:0], PSTRBF, PSTRBS, PWSTRBF, PWSTRBS
Miscellaneous Signals	HIRCOMP_x, HISWNG_x, HIVREF_x	HI_RCOMP, HI_VSWING, HI_VREF

**NOTE:** x = B, C, or D

**Table 7-3. Hub Interface 2.0 Routing Parameters**

System Type	Trace Length Min-Max (For HI2.0 Device Down)	Trace Length Min-Max (For HI2.0 Card Solution)	Trace Zo	Trace Width/Spacing	Breakout Width/Spacing
533 MHz	3" – 20"	3" – 14"	50 Ω ± 10%	5/15 mils	5/5 mils (max dist = 0.5")

The Hub Interface signals must be routed directly from the MCH to P64H2 with all signals referenced to ground. Maintain a consistent ground reference plane at all times. In addition, route all signals within a data group (consisting of nine bits of data and a pair of strobes) on the same layer and reference them to the same ground plane. Keep layer transitions to a minimum. If a layer change is required, use only two vias per net and keep all signals within a data group on the same layer.

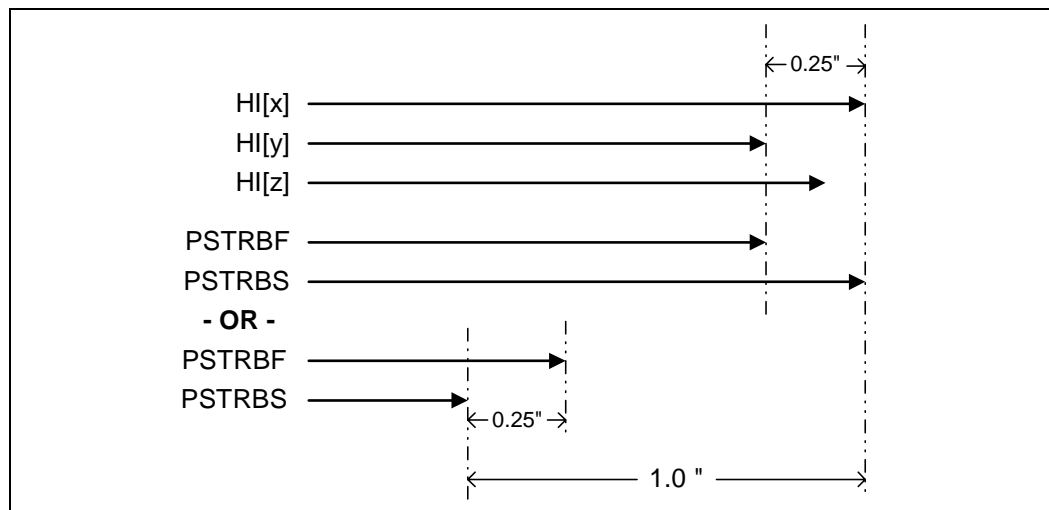
Route the Hub Interface 2.0 data signal traces 5 mils wide using the recommended stackup. There must be 15 mils spacing between signal traces (5/15). Each strobe signal must have a minimum of 35 mils of spacing from any adjacent signals to minimize effects that cause signal degradation. To break out of the MCH and P64H2 package, the hub interface data signals can be routed 5/5. The signals must separate to 5/15 (or strobes to 5/35) within 0.5 inch of the package.

Hub Interface 2.0 requires package length compensation, which is similar to the system bus package length compensation. For E7500 chipset component package lengths, refer to the component datasheets.

For Hub Interface 2.0 devices on the motherboard, package trace length matching of  $\pm 0.25$  inch (including package length compensation) is required among all signals within a data group. If the hub device is on an adapter, length matching of  $\pm 0.125$  inch (including package length compensation) is required among all signals within a data group. The hub interface strobe trace lengths must be 0 to 1.0 inch shorter than the longest hub interface data trace.

Figure 7-2 depicts the length matching rules for a hub device on the motherboard. All of the Hub Interface Data signals must be length matched within 0.25 inch. The figure shows HI[x] and HI[y] with the maximum allowed difference in length, while HI[z] is somewhere in the middle. The strobes in each strobe pair (PSTRBF and PSTRBS; PWSTRBF and PWSTRBS) are also matched within 0.25 inch. However, the absolute length of the strobe pair is adjusted according to the **longest Hub Interface Data line**. The upper pair shows the case where one of the strobes is the same **exact** length as the longest Hub Interface Data line (which is the longest possible length one of the strobes can be). In this case, the other strobe **must** be equal to or shorter than it, but by no more than 0.25 inch. The lower strobe pair shows the case where one of the strobes is **exactly** 1.0 inch shorter than the longest Hub Interface Data line (which is the shortest possible length one of the strobes can be). In this case, the other strobe **must** be equal to or longer than it, but by no more than 0.25 inch.

Figure 7-2. Hub Interface 2.0 Length matching

**NOTES:**

1. All signal lines with arrows depict the total length of the signal including the mother board trace length, MCH package trace length, and Hub Interface 2.0 device trace length.
2. PUSTRBF and PUSTRBS length matching is the same as for PSTRBF and PSTRBS.
3. This figure is only an example for an implementation with the device on the motherboard. For an implementation with the hub interface device on a riser card, simply replace both instances of 0.25" with 0.125".
4. In the example above, HI[x], HI[y], and HI[z] represent Hub Interface data signals. The other six data signals in the group must also be matched within 0.25". The associated strobe pair must be within 1.0" of the longest data signal.

Hub Interface 2.0 has a minimum trace length requirement of 3 inches, and a maximum trace length requirement of 20 inches for a device on the motherboard implementation for all hub interface signals (using an internal routing layer on the recommended stackup). However, for a device on an adapter card plugged in a hub interface 2.0 connector, the maximum motherboard trace length is 14 inches. For a riser card topology, the maximum trace length would reduce to 3 inches to (11-Y) inches, where Y is the riser card trace length. The riser must be built to not exceed the maximum trace length with the motherboard routed length.

Figure 7-3. Hub Interface 2.0 Routing Guidelines for Device Down Solutions

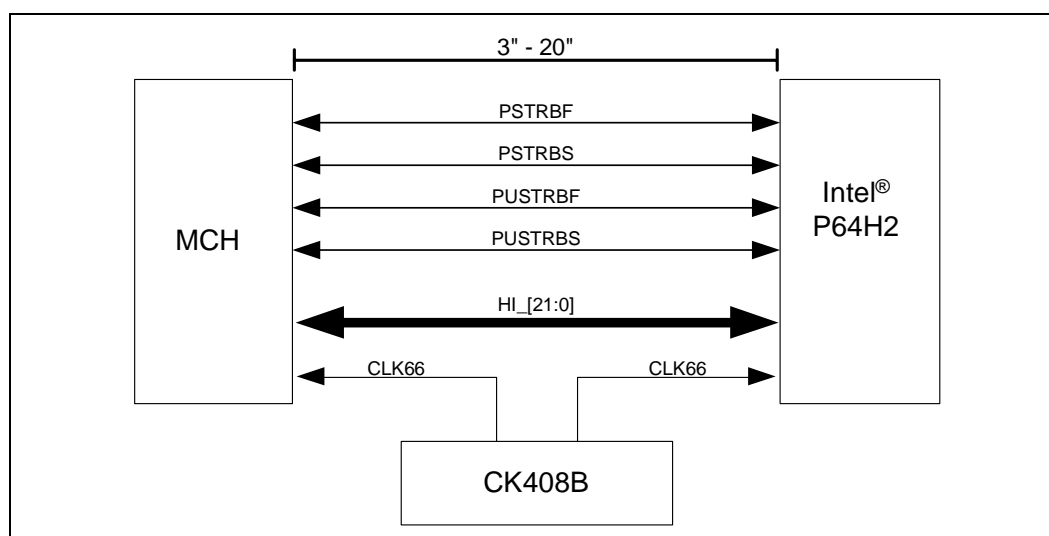
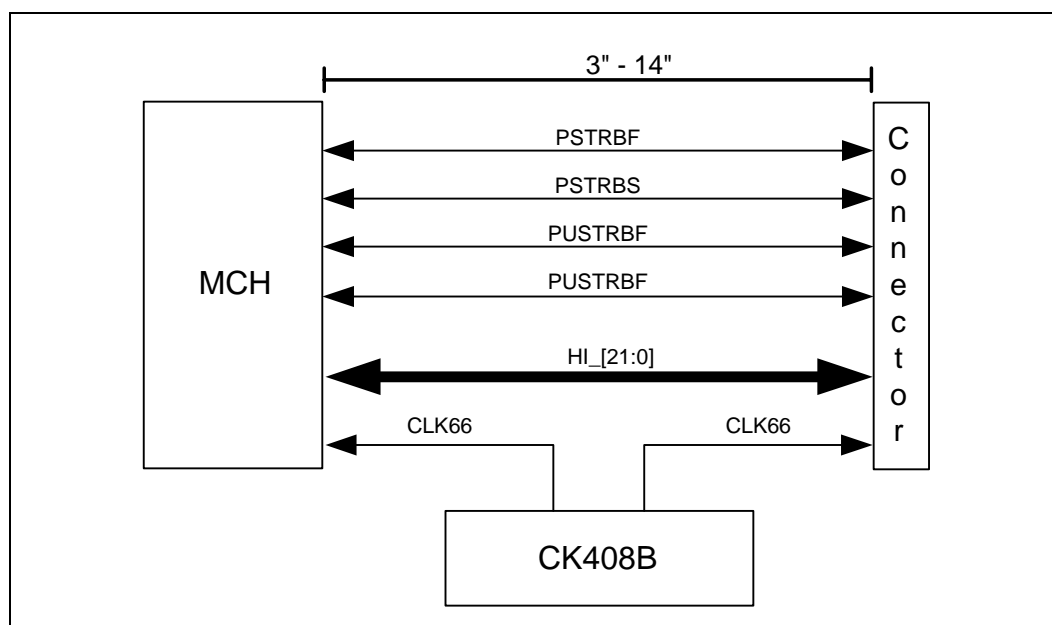


Figure 7-4. Hub Interface 2.0 Routing Guidelines for Hub Interface Connector Solutions



**NOTE:** The 14 inch maximum length allows for a single connector and 3 inch adaptor card trace length. The PCI connector is an equivalent 3 inch electrical length. The maximum motherboard trace length must be shortened if additional trace is allocated for the trace of a riser card, making sure to also subtract the additional equivalent trace of a second connector.

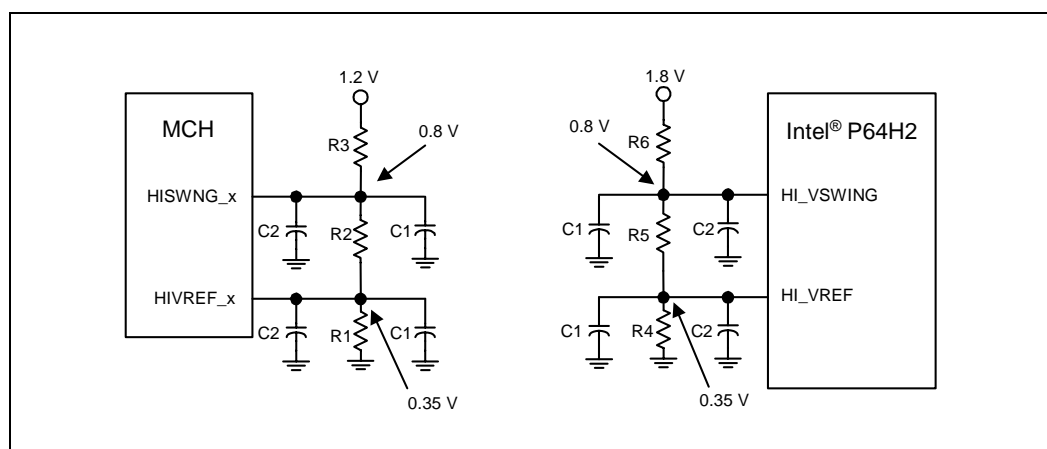
## 7.2.2 Hub Interface 2.0 Generation/Distribution of Reference Voltages

The nominal Hub Interface 2.0 reference voltage is  $0.350 \text{ V} \pm 5\%$ . Each Hub Interface 2.0 on the MCH has a dedicated HIVREF pin to sample this reference voltage. Similarly, the P64H2 has a dedicated reference voltage pin. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal Hub Interface 2.0 reference swing voltage should be  $0.8 \text{ V} \pm 5\%$  for the MCH and P64H2. Each Hub Interface 2.0 on the MCH has a dedicated HISWNG pin to sample this reference swing voltage. The P64H2 has a dedicated reference swing voltage pin as well. Both of these reference voltages can be generated locally with a single voltage divider circuit. Figure 7-5 shows an example voltage divider circuit.

Table 7-4. Hub Interface 2.0 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage Divider Circuit Recommended Resistor Values ( $\Omega$ )	1.8 V Voltage Divider Circuit Recommended Resistor Values ( $\Omega$ )
$0.350 \pm 5\%$	For P64H2 = $0.8 \pm 5\%$ For MCH = $0.8 \pm 5\%$	R1 = $392 \pm 1\%$ R2 = $499 \pm 1\%$ R3 = $453 \pm 1\%$	R4 = $261 \pm 1\%$ R5 = $332 \pm 1\%$ R6 = $750 \pm 1\%$

Figure 7-5. Hub Interface 2.0 with Locally Generated Voltage Divider Circuit



The resistor values R1, R2, R3, R4, R5, and R6 must be rated at  $\pm 1\%$  tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A  $0.1\ \mu\text{F}$  capacitor (C1 in the above circuits) should be placed close to each reference voltage divider, and a  $0.01\ \mu\text{F}$  bypass capacitor (C2 in the above circuits) should be placed near each reference voltage pin. If the length of the trace from the voltage divider to the pin is greater than 1", place more than one  $0.01\ \mu\text{F}$  capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the corresponding pin must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed 20 mils to 25 mils from all other signals.

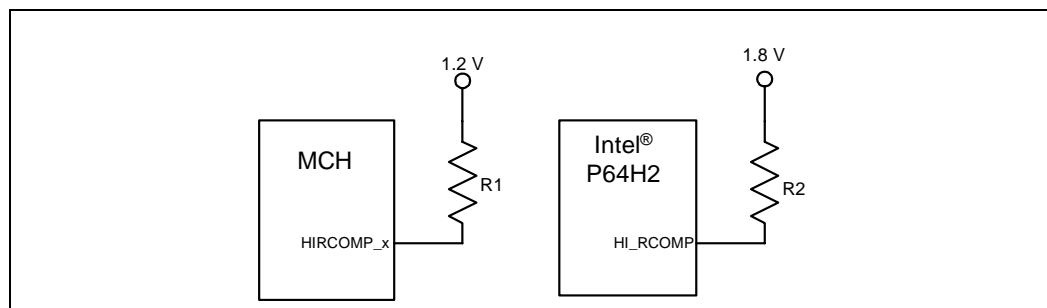
### 7.2.3 Hub Interface 2.0 Resistive Compensation

The hub interface uses a resistive compensation signal (HIRCOMP\_x) to compensate buffer characteristics across temperature, voltage, and process. The HIRCOMP\_x resistor values are given in Table 7-5. Figure 7-6 shows the RCOMP\_x circuits.

Table 7-5. Hub Interface 2.0 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	$50\ \Omega \pm 10\%$	$R1 = 24.9\ \Omega \pm 1\%$	VCC1.2
Intel® P64H2	$50\ \Omega \pm 10\%$	$R2 = 61.9\ \Omega \pm 1\%$	VCC1.8

Figure 7-6. Hub Interface 2.0 RCOMP Circuits





## 7.2.4 Hub Interface 2.0 Decoupling Guidelines

To improve I/O power delivery, use two 0.1  $\mu$ F capacitors per component (i.e., MCH, P64H2). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1.8/VCC1.2 side of the capacitors to the VCC1.8/VCC1.2 power pins. Similarly, if layout allows, metal fingers running on the VCC1.8/VCC1.2 side of the board should connect the ground side of the capacitors to the VSS power pins.

## 7.2.5 Unused Hub Interface 2.0 Interfaces

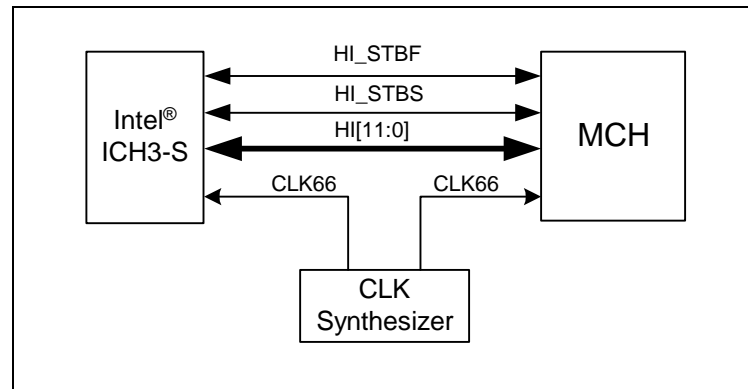
Terminate unused Hub Interface 2.0 interfaces as described below:

- All hub interface data and strobe signals can be left as no connects.
- HIVREF and HISWNG must remain connected to the reference voltage divider circuits (refer to [Figure 7-5](#)). RCOMP must be pulled up to 1.2 V.

## 7.3 Hub Interface 1.5 Implementation

The Hub Interface 1.5 signals HI[7:0] are associated with HI\_STBS/HI\_STBF. For those familiar with the Hub Interface 1.0 mode, HI\_STBF and HI\_STBS are called HI\_STB# and HI\_STB, respectively.

**Figure 7-7. 8-Bit Hub Interface 1.5 Routing**



This section documents the routing guidelines for the Hub Interface 1.5 that is responsible for connecting the MCH to the ICH3-S. Hub Interface 1.5 supports parallel termination mode only, therefore the DPRSLPVR pin on the ICH3-S must be left as No Connect (NC); this signal has an internal pull-down.

### 7.3.1 Hub Interface 1.5 High-Speed Routing Guidelines

The MCH and ICH3-S ball assignments are optimized to simplify the hub interface routing between these devices. Route the hub interface signals directly from the MCH to ICH3-S with all signals referenced to ground. Keep layer transitions to a minimum. If a layer change is required, use only two vias per net, and keep all data signals and associated strobe signals on the same layer.

The Hub Interface 1.5 signal groups are listed in [Table 7-6](#). The general routing guidelines for the Hub Interface 1.5 signals are given in [Table 7-7](#).

Table 7-6. Hub Interface 1.5 Signal Groups

Group	Signals	
	MCH	Intel® ICH3-S
Common Clock Signals	HI_A[11:8]	HI[11:8]
Source Synchronous Signals	HI_A[7:0], HI_STBF, HI_STBS	HI[7:0], HI_STBF, HI_STBS
Miscellaneous Signals	HIRCOMP_A, HISWNG_A, HIVREF_A	HICOMP, HITERM, HIREF

Table 7-7. Hub Interface 1.5 Routing Parameters

System Type	Trace Length Min-Max	Trace $Z_0$	Trace Width/Spacing	Breakout Width/Spacing
266 MHz	3" – 20"	50 $\Omega \pm 10\%$	5/15 mils	5/5 mils (max dist = 0.3")

Using the recommended stackup, the Hub Interface 1.5 data signal traces must be routed 5 mils wide. There must be 15 mils spacing between traces (5/15). To break out of the MCH and ICH3-S packages, the Hub Interface data signals can be routed 5/5. The signals must be separated to 5/15 within 0.3 inch of the package.

For Hub Interface 1.5 devices on the motherboard, each strobe signal trace must be the same length, and each data signal trace must be matched within  $\pm 0.1$  inch.

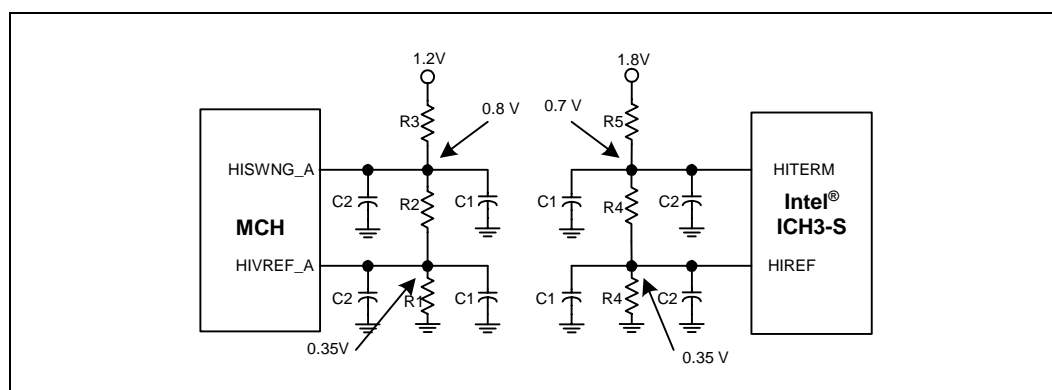
### 7.3.2 Hub Interface 1.5 Generation/Distribution of Reference Voltages

The nominal Hub Interface 1.5 reference voltage is  $0.35 \text{ V} \pm 5\%$ . The 8-bit Hub Interface on the MCH has a dedicated HIVREF pin to sample this reference voltage. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal Hub Interface 1.5 reference voltage swing must be  $0.8 \text{ V} \pm 5\%$  for the MCH and  $0.7 \text{ V} \pm 5\%$  for the ICH3-S. This voltage is sampled by the MCH using HISWNG, and is sampled by the ICH3-S using HITERM. (see Table 7-8). Both HISWNG and HITERM can be generated locally with a single voltage divider circuit as shown in Figure 7-8.

Table 7-8. Hub Interface 1.5 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage Divider Circuit Recommended Resistor Values ( $\Omega$ )	1.8 V Voltage Divider Circuit Recommended Resistor Values ( $\Omega$ )
$0.35 \pm 5\%$	For ICH3-S = $0.7 \pm 5\%$ For MCH = $0.8 \pm 5\%$	R1 = $392 \pm 1\%$ R2 = $499 \pm 1\%$ R3 = $453 \pm 1\%$	R4 = $261 \pm 1\%$ R5 = $825 \pm 1\%$

Figure 7-8. Hub Interface 1.5 Locally Generated Reference Divider Circuits



The values of R1, R2, R3, R4 and R5 must be rated at  $\pm 1\%$  tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A  $0.1\ \mu\text{F}$  capacitor (C1 in Figure 7-8) should be placed within 0.5 inch of each resistor divider, and a  $0.01\ \mu\text{F}$  bypass capacitor (C2 in Figure 7-8) should be placed within 0.25 inch of reference voltage pins. If the length of the trace from the voltage divider to the pin is greater than 1 inch, place more than one  $0.01\ \mu\text{F}$  capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the HIREF and HUBREF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 20 mils to 25 mils from all other signals.

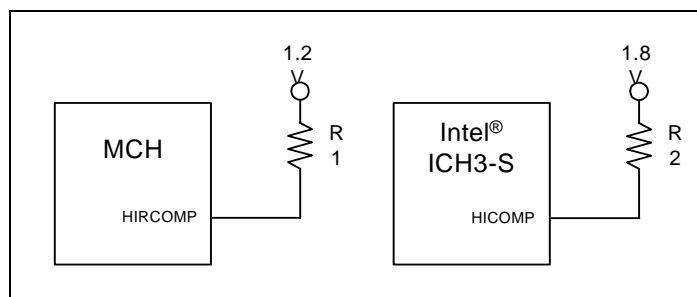
### 7.3.3 Hub Interface 1.5 Resistive Compensation

The hub interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process. The HIRCOMP resistor values are given in Table 7-9. Figure 7-7 shows the RCOMP\_x circuits.

Table 7-9. Hub Interface 1.5 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	$50\ \Omega \pm 10\%$	$R1 = 24.9\ \Omega \pm 1\%$	VCC1.2
ICH3-S	$50\ \Omega \pm 10\%$	$R2 = 78.7\ \Omega \pm 1\%$	VCC1.8

Figure 7-9. Hub Interface 1.5 RCOMP Circuits



### 7.3.4 Hub Interface 1.5 Decoupling Guidelines

To improve I/O power delivery, use two 0.1  $\mu$ F capacitors per each component (i.e., the ICH3-S and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC\_1.8/VCC\_1.2 side of the capacitors to the VCC\_1.8/VCC\_1.2 power pins. Similarly, if layout allows, metal fingers running on the VCC\_1.8/VCC\_1.2 side of the board should connect the ground side of the capacitors to the VSS power pins.

# Intel® 82870P2 (P64H2)

## 8

The 82870P2 (P64H2) is a peripheral chip that performs PCI/PCI-X bridging functions between Hub Interface and the PCI bus. The P64H2 is an integral part of the E7500 chipset, bridging the MCH and the PCI/PCI-X bus. On the primary bus, the P64H2 utilizes a 16-bit data bus to interface with the Hub Interface 2.0, and on the secondary bus, it supports two 64-bit PCI bus segments. Either of the secondary PCI/PCI-X bus interfaces can be configured to operate in PCI or PCI-X mode. Each PCI/PCI-X interface contains an I/OxAPIC with 24 interrupts and a hot plug controller that supports each PCI/PCI-X bus segment.

## 8.1 PCI/PCI-X Design Guidelines

The P64H2 contains two PCI/PCI-X Interfaces. The PCI Interface has a 33/66 MHz bus speed, and the PCI-X interface has a 66/100/133 MHz bus speed (see [Table 8-1](#)).

**Table 8-1. PCI/PCI-X Frequencies**

PCI		
Frequency	Maximum Slots	Voltage
33 MHz	6	3.3 V, 5 V
66 MHz	2	3.3 V

PCI-X		
Frequency	Maximum Slots	Voltage
66 MHz	4	3.3 V
100 MHz	2	3.3 V
133 MHz	1	3.3 V

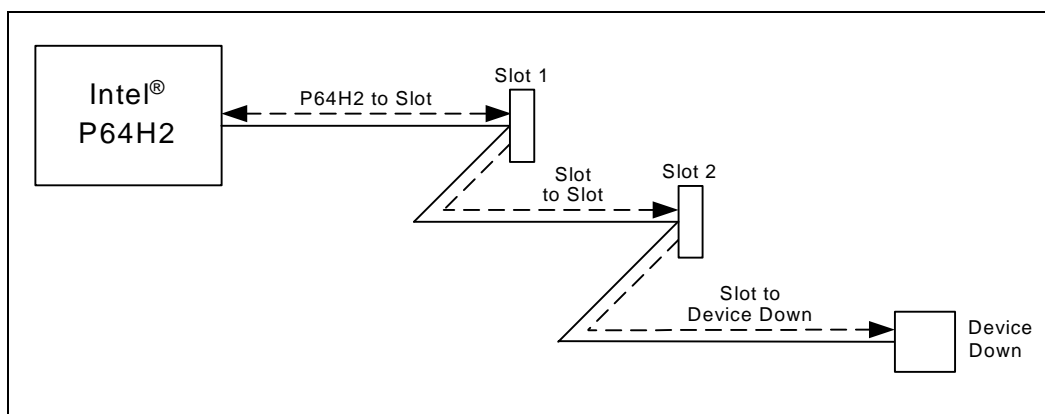
**NOTE:** Frequencies specified are not the only ones supported, rather the maximum allowed in the configuration.

Intel simulated the PCI/PCI-X bus topologies shown in [Section 8.1.1](#) and [Section 8.1.2](#). If a platform implements a PCI/PCI-X topology not found in the following sections, it is the responsibility of the system designer to ensure the system meets the specified timings. The recommended lengths specified are not intended to replace thorough system simulations and validation.

### 8.1.1 PCI/PCI-X Routing Requirements (No Hot Plug)

The P64H2 supports a large number of PCI/PCI-X configurations. The basic topology of the bus is shown in [Figure 8-1](#). Multiple slots are connected in a daisy chain topology with the device(s) down on the motherboard at the end of the daisy chain. [Table 8-2](#) documents the lengths for the configurations Intel simulated.

**Figure 8-1. Typical PCI/PCI-X Routing**



**Table 8-2. Intel® P64H2 PCI/PCI-X Configuration Length Requirements**

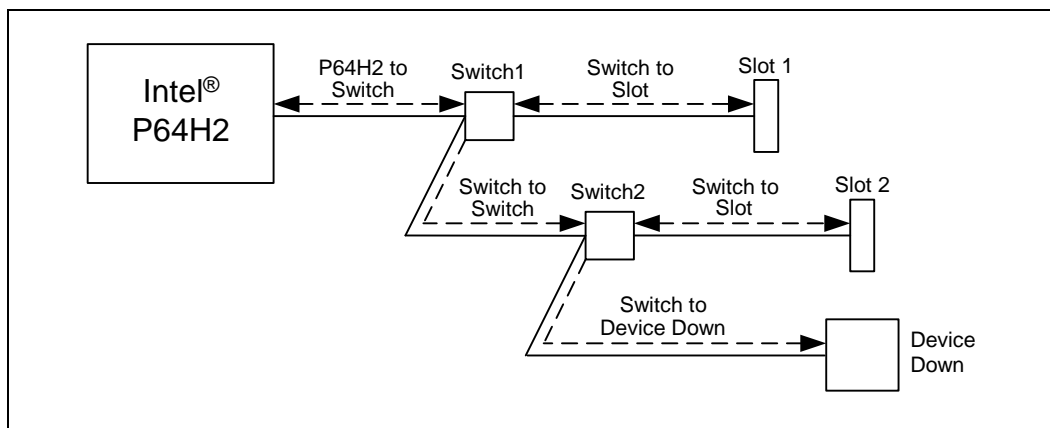
Configuration	Intel® P64H2 to Slot	Slot to Slot	Slot to Device Down
33 MHz, 5 slots / 1 device down	2.0" – 7.0"	1.0"	3.0" – 6.0"
66 MHz, 4 slots / 0 devices down	6.0" – 8.0"	1.5"	N/A
100 MHz, 2 slots / 0 devices down	5.0" – 8.0"	1.0" – 1.75"	N/A
100 MHz, 2 slots / 1 device down	3.0" – 3.5"	0.75"	2.5" – 3.0"
100 MHz, 1 slot / 2 devices down	2.0" – 4.0"	(device to device) 2.0"	5.0"
133 MHz, 1 slot / 0 devices down	1.0" – 6.0"	N/A	N/A

**NOTE:** During simulation, slot to slot lengths were held constant for some configurations. Therefore, no range can be given for these length requirements.

## 8.1.2 PCI/PCI-X Hot Plug Routing Requirements

The P64H2 supports a large number of PCI/PCI-X Hot Plug configurations. The Hot Plug topology of the bus is shown in Figure 8-2. Hot Plug switches are connected in a daisy chain topology with the device(s) down on the motherboard at the end of the daisy chain. Table 8-3 documents the lengths for the configurations that Intel simulated.

**Figure 8-2. Typical Hot Plug Routing**



**Table 8-3. Intel® P64H2 Hot Plug Configuration Length Requirements**

Configuration	Intel® P64H2 to Switch	Switch to Slot	Switch to Switch	Switch to Device Down
66 MHz, 4 Slots / 0 Device	2.0" – 6.0"	0.5" – 3.0"	0.5"	N/A
100 MHz, 2 Slots / 1 Device	2.5" – 3.5"	0.5" – 0.75"	0.75"	1.5" – 2.5"
100 MHz, 2 Slots / 0 Device	3.5" – 4.5"	1.0" – 1.75"	1.0" – 1.75"	N/A
100 MHz, 1 Slot / 1 Device	4.0" – 5.0"	1.75" – 2.25"	N/A	3.5" – 4.5"
133 MHz, 1 Slot / 0 Devices	1.5" – 3.5"	0.5" – 3.0"	N/A	N/A

**NOTE:** During simulation, slot to slot lengths were held constant for some configurations. Therefore, no range can be given for these length requirements.

### 8.1.3 Clock Configuration

All PCI clocks must be disabled in the BIOS for any unused/unpopulated PCI/PCI-X slots. The P<sub>x</sub>PCLKO[5:0] pins can each be disabled by writing to the Disable PCLKOUT 5 – 0 bits (DPCLK, bits 15:10, config register offset 40h in each bridge). These clocks function the same in Serial and 2-Slot Parallel modes. In 1-Slot Serial Mode, the P<sub>x</sub>PCLKO[5:0] signals are all driven low when the clock to the slot is disabled by the hot plug controller, regardless of the DPCLK bits. Once the Hot Plug controller connects the clock to the slot, these clocks are enabled again—which clocks are enabled does depend on DPCLK at this point. It is expected that P<sub>x</sub>PCLK[0] will be connected to the PCI slot in Single Slot Parallel Mode.

Figure 8-3. Hot Plug Clock Configuration

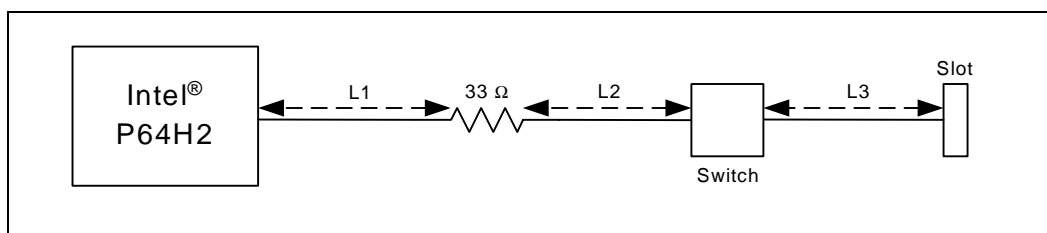


Table 8-4. Hot Plug Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches)	L3 (inches)
66 MHz	0.25 – 1.0	$(L_{fbi} - L3) - 2.523$	0.75 – 1.25
100 MHz	3.5 – 4.5	$0.25 - 0.5 = L3$	$0.25 - 0.5 = L2$
133 MHz	1.5 – 2.5	$0.5 - 1.0 = L3$	$0.5 - 1.0 = L2$

Figure 8-4. No Hot Plug Clock Configuration

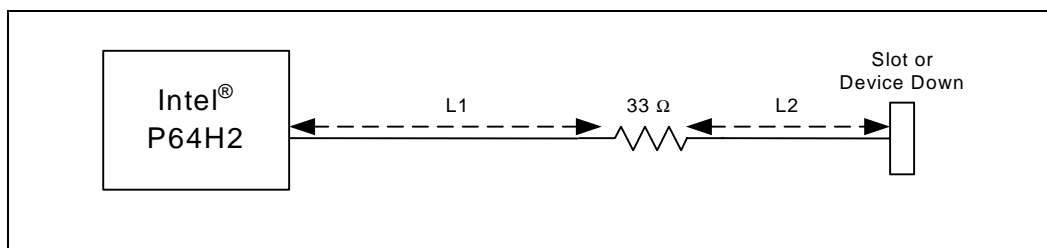


Table 8-5. No Hot Plug Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches) Slot	L2 (inches) Device Down
33 MHz Slot	3.5 – 5.5	0.5 – 5.0	2.9 – 7.9
66 MHz	3.5 – 4.5	0.5 – 1.0	3.0 – 3.5
100 MHz	$\leq 1.0$	$L_{fbi} - 2.5^1$	$L_{fbi}^1$
133 MHz	$\leq 1.0$	$L_{fbi} - 2.5^1$	$L_{fbi}^1$

**NOTES:**

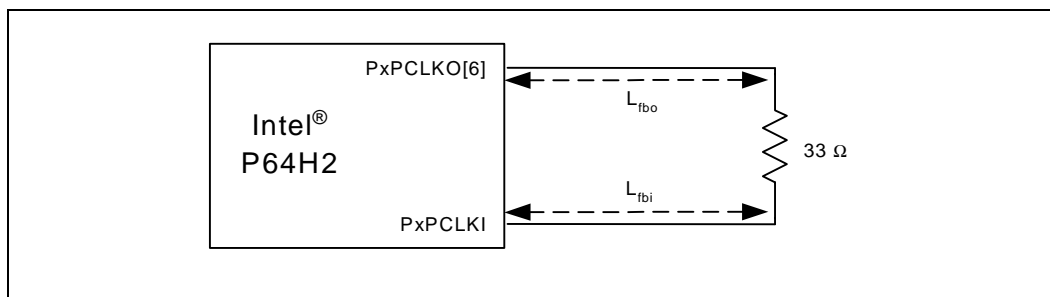
1. The clock signal and feedback loops are closely related. Refer to Figure 8-4 for L2, and Figure 8-5 for  $L_{fbi}$ .



## 8.1.4 Loop Clock Configuration

You must tie PxPCLKO[6] to PxPCLKI because this clock always runs and is needed by the internal PCI PLLs to properly align output signals with the external clocks by removing clock insertion delay. The PxPCLKO[6] signal does not have to be routed through a bus switch before returning to PxPCLKI.

**Figure 8-5. Loop Clock Configuration**



**Table 8-6. Loop Clock Configuration Routing Length Parameters**

Clock Speed / Config	$L_{fbo}$ (inches)	$L_{fbi}$ (inches)
33 MHz / No HP	3.5 – 5.5	2.9 – 7.9
66 MHz / No HP	4.5 – 5.5	3.9 – 4.9
66 MHz / With HP	0.25 – 1.0	7.0 – 12.0
100 MHz / No HP	$\leq 1.0$	$L2 + 2.5^1$
100 MHz / With HP	4.5 – 5.5	3.9 – 4.9
133 MHz / No HP	0.25 – 1.0	$L2 + 2.5^1$
133 MHz / With HP	3.5 – 4.0	5.5 – 5.7

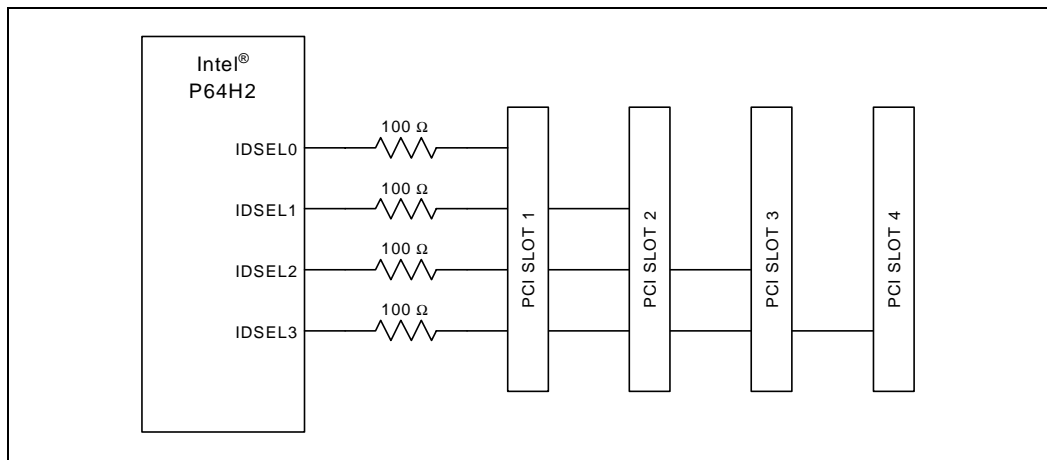
**NOTES:**

1. The clock signal and feedback loops are closely related. Refer to [Figure 8-4](#) for L2 and [Figure 8-5](#) for  $L_{fbi}$ .

### 8.1.5 IDSEL Implementation

Designers should use a 100  $\Omega$  series coupling resistor on the IDSEL signal when implementing PCI-X. Though the *PCI-X Addendum PCI Local Bus Specification, Revision 1.0* calls for a 2 k $\Omega$  resistor, the current specification, *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a* allows for other resistor values. See Figure 8-6 for an example of how to implement the coupling resistor. IDSEL mapping per P64H2 pin is arbitrary. However, AD16 is reserved.

Figure 8-6. IDSEL Sample Implementation Circuit



### 8.1.6 SMBus Address

The SMBus interface does not have configuration registers. The SMBus address is set by the states of pins PA\_GNT[5:4] and PB\_GNT[5:4] when PWROK is asserted as described in Table 8-7. Refer to the *Intel® PCI-64 Hub 2 (P64H2) Datasheet* for a more detailed description of P64H2 strap latching.

Table 8-7. SMBus Address Configuration

Bit	Value
7	1
6	1
5	PA_GNT[5]
4	0
3	PA_GNT[4]
2	PB_GNT[5]
1	PB_GNT[4]

**NOTE:** There is no bit 0 because it is the read/write direction indicator.

## 8.2 Hot Plug Implementation

The P64H2 contains two integrated Hot Plug Controllers (one per PCI/PCI-X interface) that operate independently. These integrated controllers can be individually disabled or configured to operate in one of the three defined modes of operation: Single Slot Parallel mode, Dual Slot Parallel mode, and Serial mode. This section describes each of these three modes of operation, as well as switch and button implementation and the Hot Plug Standard Usage Model.

### 8.2.1 Standard Usage Model

To define a programming model for the Hot Plug Controllers (HPC), it is necessary to make some assumptions about the interface between a user and a Hot Plug system that must be incorporated into the hardware solution. The programming model includes two LED indicators, one optional push button, and a sensor on the manually-operated retention latch (MRL) for each supported slot. See [Section 8.2.2](#) for MRL and attention button implementation. [Section 8.2.3](#) describes the LED indicators. For more information on the standard usage model, see the *PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0*.

**Caution:** Users must always notify the operating system via a software user interface or Attention Button (if present) before opening an MRL. This allows the operating system to isolate the slot from the PCI bus and unload the device driver gracefully. The unexpected opening of an MRL leads to unpredictable results, including data corruption, abnormal termination of the operating system, or damage to card or platform hardware.

#### 8.2.1.1 Hot-Removals

1. User selects a slot holding an enabled add-in card and requests that slot be disabled.
  - a. User interacts with a software user interface to request that slot be disabled.
  - b. User confirms request. System software validates request and initiates slot power down sequence. Power Indicator LED blinks.

-- OR --

  - a. User presses momentary Attention Button at that slot.
  - b. Software interprets change on HxPRSNT# pin as a push button event. (Software ignores second interrupt on HxPRSNT# caused by button release.) Power Indicator LED blinks.
  - c. User is permitted to cancel request within 5 seconds by pressing Attention Button again.
  - d. System software validates request and initiates slot power down sequence.
2. System software waits for card activity on the PCI bus to end.
3. Hot Plug Controller asserts RST#, bus signals and clock lines are disconnected from the slot, and power is removed.
4. Power Indicator LED is turned off. User may open MRL, disconnect cables, and remove card.

### 8.2.1.2 Hot-Insertions

1. User selects an empty, disabled slot and opens MRL.
2. User inserts add-in card, closes MRL, and attaches cables to card.
3. User requests that slot be enabled.
  - a. User requests that slot be enabled via a software user interface.
  - b. Power Indicator LED next to slot blinks while system software validates request.

-- OR --

- a. User presses momentary Attention Button at that slot.
  - b. Software interprets change on HxPRSNT# pin as a push button event. (Software ignores second interrupt on HxPRSNT# caused by button release.)
  - c. User is permitted to cancel request within 5 seconds by pressing Attention Button again.
  - d. Power Indicator LED next to slot blinks while system software validates request.
4. Hot Plug Controller asserts RST# to the slot; main supply voltages are present at the slot.
5. Clock and bus signals are connected to the slot; RST# is deasserted.
6. Power Indicator LED is turned on. The slot is ready for operation.

## 8.2.2 Hot Plug Switch Implementation

The mechanical design for the chassis should include a manually-operated retention latch (MRL) that holds an add-in card in the slot. Each MRL should have an associated switch, optical device, or other type of sensor to indicate whether a slot is “opened” or “closed.” (Note that the terms opened and closed do not necessarily indicate the electrical state of the switches used, but should be thought of as a mechanical door that enables or disables cards to be installed or removed.) A slot can be auto-powered down should someone attempt to remove a card without first notifying the operating system. The mechanical design should be such that it is impossible for an expansion card to be removed without the switch indicating that the slot is open. The mechanical design should also prevent inadvertent switch “openings.”

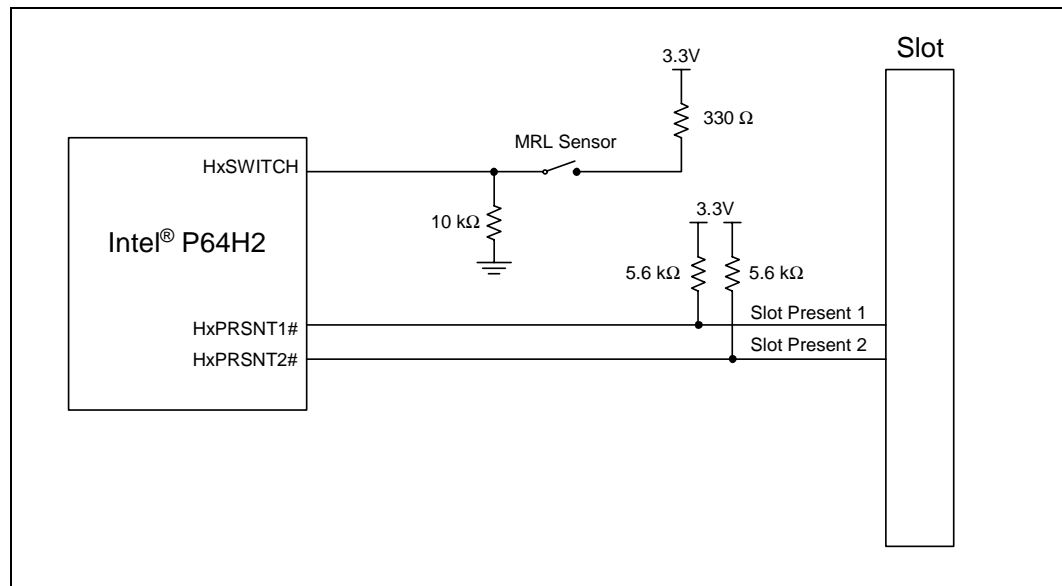
An Attention Button is a momentary-contact push-button. This button serves to invoke the hot-plug service so that an adapter can be added or removed without the use of a software interface. Support for the Attention Button is optional.

### 8.2.2.1 Manually-Operated Retention Latch Sensor

The HxSWITCH signal is monitored by the Hot Plug Controller to determine whether or not a slot should be powered. The MRL sensor, or slot switch, should be connected to the HxSWITCH pin such that it drives this pin low to indicate that the slot is closed and can be powered on. When the signal is driven high, it indicates that the slot should immediately be powered off. The MRL Sensor is represented schematically as a switch in Figure 8-7.

The Slot Present pins on each hot-plug slot are connected directly to the HxPRSNT1# and HxPRSNT2# pins on the P64H2.

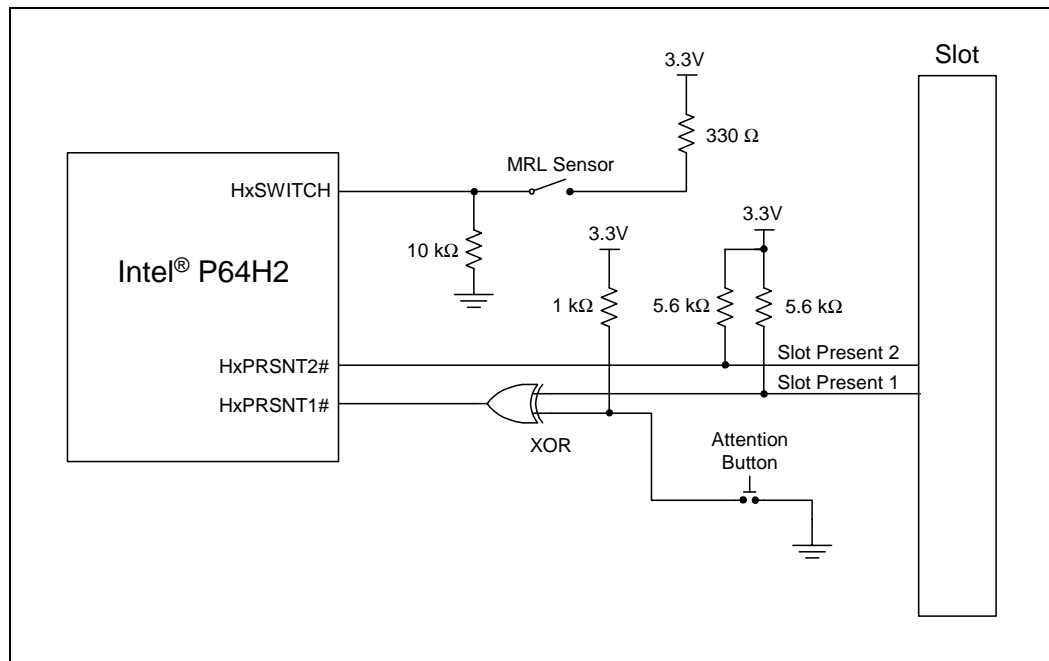
**Figure 8-7. Manually-Operated Retention Latch Sensor**



### 8.2.2.2 Optional Attention Button

The Attention Button state is observed on the slot-specific HxPRSNT1# pin. An exclusive-OR (XOR) gate is inserted between the Slot Present signal and the Hot Plug Controller as shown in Figure 8-8. A momentary contact button is connected to the other input of the XOR gate. When the button is in the released state, the Slot Present signal is unaffected. When the button is actively being pressed/asserted, the Slot Present signal is inverted, signaling the Hot Plug Controller to commence slot power up/down sequence.

Figure 8-8. Attention Button Implementation



### 8.2.3 LED Indicator Outputs

The PCI Hot-Plug Standard Usage Model assumes that the Platform provides two indicators per slot. Indicators must be placed in close proximity to their associated slot so that the association between the indicators and the hot-plug slot is clear.

The LED output signals for all modes of P64H2 Hot Plug Controller operation are active high. In all cases, the green LED is the power indicator, and the amber LED is the attention indicator.

## 8.2.4 Disabling/Enabling an Intel® P64H2 Hot Plug Controller

### 8.2.4.1 Hot Plug Strapping Options

The HPxSLOT [2:0] strapping pins are used to enable and disable the Hot Plug Controller. [Table 8-8](#) lists the strapping options associated with these pins, and the modes of operation they enable.

**Table 8-8. Hot Plug Mode**

HPxSLOT [2:0]	Hot Plug Mode	Notes
000	Hot Plug Disabled	
001	1-Slot (Parallel Mode)	1
010	2-Slot (Parallel Mode)	2
011	3-Slot (Serial Mode)	3
100	4-Slot (Serial Mode)	3
101	5-Slot (Serial Mode)	3
110	6-Slot (Serial Mode)	3
111	Reserved	

**NOTES:**

1. Refer to [Section 8.2.5](#) for Single Slot Parallel Mode Operation.
2. Refer to [Section 8.2.6](#) for Dual Slot Parallel Mode Operation.
3. Refer to [Section 8.2.6.9](#) for Serial Mode Operation.

### 8.2.4.2 Hot Plug Registers' Visibility

The Hot Plug controller function is completely hidden when the controller is disabled by the slot strapping pins HPx\_SLOT[2:0], and the registers are not available or accessible.

## 8.2.5 Single Slot Parallel Mode

Single Slot Parallel Mode allows for only one card to be connected to the PCI/PCI-X Bus. This mode should be used only to implement a one-slot Hot Plug solution because of the behavior of the PCI bus when in this mode. No serialization/deserialization logic is required for this mode of operation.

### 8.2.5.1 Required Additional Logic

Single Slot Parallel Mode requires a power switch to be used to turn the slot power on and off. Single Slot Parallel Mode does not require the use of a bus and clock switch. In this mode, all PCI signals are driven to ground whenever a PCI card is to be disconnected.

If the platform supports PME# or SMBus connections to the slot, isolation logic is required to disconnect these signals prior to inserting or removing a card. See the *PCI Hot Plug Specification, Revision 1.1* for implementation details. The Hx\_SWITCH signal can be used to control the isolation switches.

### 8.2.5.2 PCI Clock

In Single Slot Parallel Mode, it is expected that PxPCLK [0] is used.

### 8.2.5.3 Debounced Hot Plug Switch Input

The switch inputs (Px\_IRQ[15] in this case—see [Table 8-10](#)) to the Hot Plug controller do not require any debouncing logic in this mode. This logic is contained within the P64H2. The POWERON value for this input is determined by BIOS. However, it is recommended that BIOS define a logic 0 to represent that the slot can be powered on.

### 8.2.5.4 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification, Revision 2.2* for this circuit. For more information on the reference circuit, refer to [Section 8.2.6.9](#). The Board Designers could also use [Table 8-9](#) as a reference.

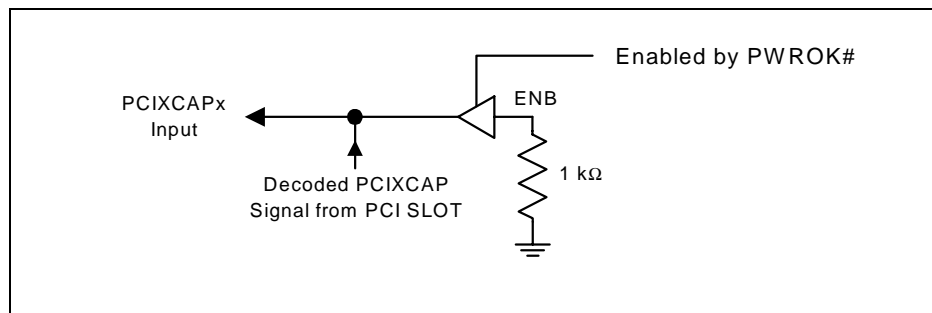
**Table 8-9. Frequency Matrix**

Frequency	M66EN	PCIXCAP1	PCIXCAP2	133EN
PCI 33	0	X	X	X
PCI 66	1	0	0	X
PCI-X 66	X	1	0	X
PCI-X 100	X	1	1	0
PCI-X 133	X	1	1	1

### 8.2.5.5 Tri-State Buffer or 2:1 MUX for HPxSLOT [2:0]

The HPxSLOT [2:0] pins are pull-ups/pull-downs for determining the slot count and mode of operation for the P64H2 Hot Plug Controller. The strapping value on these pins is latched on the rising edge of PWROK. In Single Slot Parallel Mode, these pins also function as the PCIXCAP1A, PCIXCAP2A, and PCIXCAP1B inputs to the controller. Logic must exist to preserve the slot count value when the system is in reset (PWROK signal is low).

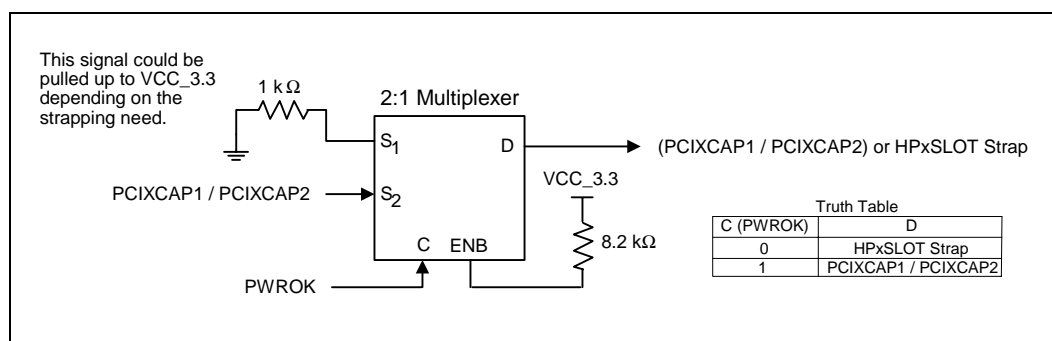
**Figure 8-9. Tri-State Buffer Circuit Example**



It is also possible to accomplish this strapping requirement using a 2:1 MUX. The PWROK signal can be used to enable the tri-state buffer. The decision is left up to the individual designer on which method to use. See [Figure 8-10](#) for an example of the optional MUX circuit.



Figure 8-10. MUX Circuit Example



## 8.2.5.6 Hot Plug Muxed Signals in Single Slot Parallel Mode

The Hot Plug signals that connect to the controller are as follows:

Table 8-10. Single Slot Parallel Mode Hot Plug Signal Table

Signal	Type	Muxed With				Note
		Bus A	Ball #	Bus B	Ball #	
HxSWITCHA	I	PA_IRQ[15]	F4	PB_IRQ[15]	F1	
HxFAULTA#	I	PA_IRQ[14]	E4	PB_IRQ[14]	E1	
HxPRSNT2A#	I	PA_IRQ[13]	F5	PB_IRQ[13]	D1	
HxPRSNT1A#	I	PA_IRQ[12]	E5	PB_IRQ[12]	C1	
HxM66ENA	I/O	PA_IRQ[11]	D5	PB_IRQ[11]	B1	
HxPCIXCAP1A	I	HPA_SLOT[2]	D20	HPB_SLOT[2]	D23	1
HxPCIXCAP2A	I	HPA_SLOT[1]	C20	HPB_SLOT[1]	C23	1
HxRESETA#	O	PA_GNT[5]	E22	PB_GNT[5]	G4	2
HxGNLEDA	O	HPA_SOC	A19	HPB_SOC	A24	2
HxAMLEDA	O	HPA_SOL	D19	HPB_SOL	C22	2
HxBUSENA#	O	HPA_SORR#	A18	HPB_SORR#	A22	2, 3
HxCLKENA#	O	HPA_SIL#	D24	HPB_SIL#	D24	2, 3
HxPWRENA	O	HPA_SOD	B19	HPB_SOD	C24	2

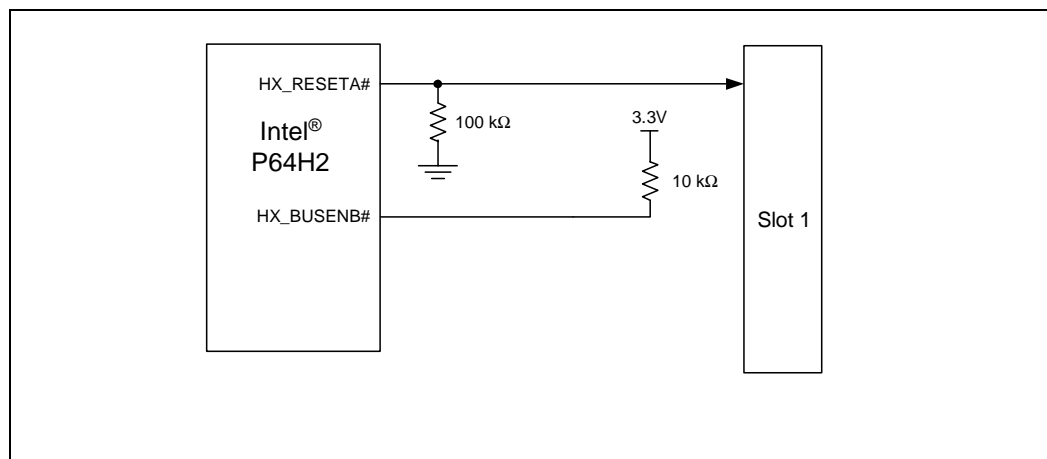
1. HPx\_SLOT [N] are pull-ups/pull-downs. When in dual slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. The P64H2 must drive this signal to its corresponding state shown in Table 8-11 in case the system is set up for single slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the P64H2 in dual slot parallel mode is the same value it would have driven if in serial mode.
3. In parallel mode, the BUSENA# and CLKENA# signals become active low instead of active high as they are during serial mode.

**Table 8-11. Hot Plug Controller Output Signal Reset Values**

Signals	Reset Value
Px_GNT[5:3]	011
HPx_SOC	0
HPx_SIC	0
HPx_SOL	0
HPx_SOLR	0
HPx_SOD	0
HPx_SORR#	1
HPx_SOR#	0
HPx_SIL#	1

### 8.2.5.7 SMBus Address Considerations

In Single Slot Parallel mode, the SMBus address strap pins listed in [Table 8-7](#) are muxed with Hot Plug control signal HxRESETA#. Therefore, it is recommended that the following technique be used for determining an SMBus address. Pull the PA\_GNT5 (RESETA#) signal to ground through a  $100\text{ k}\Omega \pm 5\%$  resistor. This will keep the reset signal active until the P64H2 is ready for it to become deasserted. Pull the PA\_GNT4 (Hx\_BUSENB#) signal to 3.3 V through a  $10\text{ k}\Omega \pm 5\%$  resistor. The P64H2 will be able to drive this signal to ground when the signal must be asserted.

**Figure 8-11. Single Slot Parallel SMBus Circuit**

### 8.2.5.8 Pull-Ups/Pull-Downs in Single Slot Parallel Mode

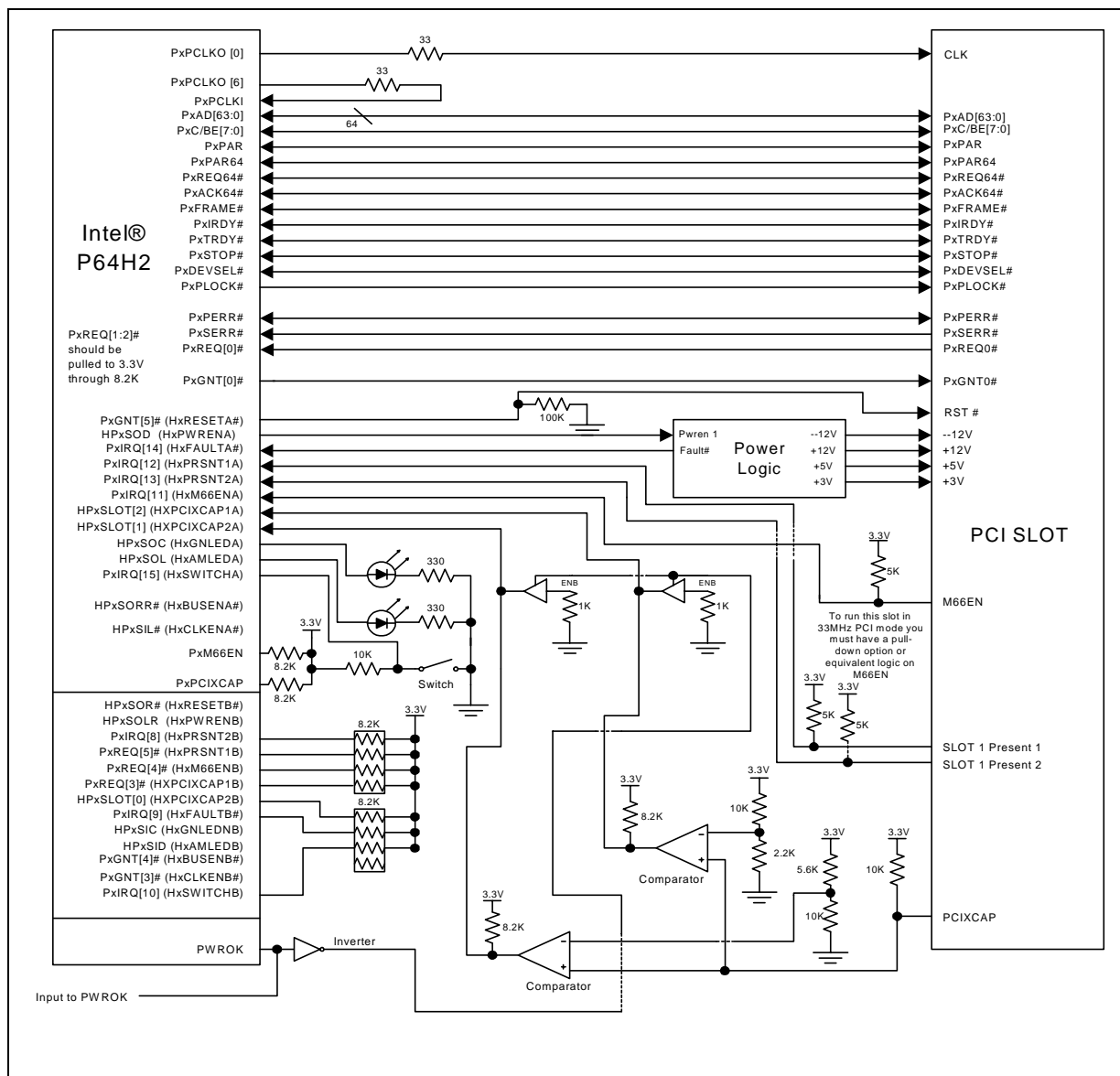
All PCI signals should follow the *PCI Local Bus Specification, Revision 2.2* pull-up requirements whether they are muxed or not. All unused input signals should be pulled to 3.3 V through an  $8.2\text{ k}\Omega \pm 5\%$  resistor to keep them from floating.

[Table 8-10](#) defines which muxed signals are to be used with single slot mode. Note that whether in single or dual slot mode, all signals from [Table 8-10](#) are actually muxed even though only the signals listed in [Table 8-11](#) are used. As a result, all unused input signals listed in [Table 8-10](#) must be pulled to 3.3 V through an  $8.2\text{ k}\Omega \pm 5\%$  resistor to keep them from toggling.

### 8.2.5.9 Reference Schematic for Single-Slot Parallel Mode

Note that the following schematics are based on definition and simulation of the P64H2. These schematics have not been fully validated.

**Figure 8-12. Reference Schematic for Single-Slot Parallel Mode**



## 8.2.6 Dual Slot Parallel Mode

Dual Slot Parallel Mode is used when it is desirable to have two slots that are Hot Pluggable. No serialization/deserialization logic is required for this mode of operation.

### 8.2.6.1 Required Additional Logic

Dual Slot Parallel Mode requires a power switch to be used to turn the slot power on and off. Dual Slot Parallel Mode also requires the use of a bus and clock switch. Unlike single slot parallel mode, the PCI signals are not driven to ground whenever a PCI card is to be disconnected. In addition, Dual Slot Parallel Mode requires auto bus and clock disable logic to immediately disable the PCI bus and clock when the power fault signal (from the power switch) goes active.

If the platform supports PME# or SMBus connections to the slots, isolation logic is required to disconnect these signals before inserting or removing a card. See *PCI Hot Plug Specification, Revision 1.1* for implementation details.

### 8.2.6.2 Debounced Hot Plug Switch Input

The switch inputs (PA\_IRQ[15] and PA\_IRQ[10] in this case—see [Table 8-12](#)) to the Hot Plug controller do not require debouncing logic in this mode. This logic is contained within the P64H2.

### 8.2.6.3 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification, Revision 2.2* for this circuit. An example of this circuit is also contained in the reference schematics. For a frequency reference matrix, see [Table 8-9](#).

### 8.2.6.4 Tri-State Buffer or 2:1 Mux for HPxSLOT [2:0]

As with Single Slot Parallel Mode, the HPxSLOT [2:0] pins are pull-ups/pull downs for determining the slot count and mode of operation for the P64H2 Hot Plug Controller in Dual Slot Parallel Mode. The strapping value on these pins is latched on the rising edge of PWROK. In Dual Slot Parallel Mode these pins also function as the PCIXCAP1A, PCIXCAP2A, and PCIXCAP1B inputs to the controller. Logic must exist to preserve the slot count value when the system is in reset (PWROK signal is low). Connecting a tri-state buffer or a 2:1 MUX to these pins to pull the line high or low accordingly can do this. The PWROK signal can be used to enable the tri-state buffer to drive the line high or low or select the MUX signal. See [Figure 8-9](#) for a tri-state buffer example circuit, and [Figure 8-10](#) for a 2:1 MUX circuit example.

### 8.2.6.5 HPx\_SID Output Signal

In Dual Slot Parallel Mode, this signal is connected to the Amber LED slot status indicator. During a reset operation, this signal goes high which could flicker the LED on and confuse the user. To avoid having this LED turn on during a reset operation (PWROK logic zero), it is possible to use a buffer to electrically isolate this LED from the HPx\_SID signal. The PWROK input signal to the P64H2 should be used to enable this buffer. See the Dual Slot Mode reference schematic in [Section 8.2.6.9](#) for an example of this circuit.

### 8.2.6.6 Pull-Ups/Pull-Downs in Dual Slot Parallel Mode

All PCI signals should follow the *PCI Local Bus Specification, Revision 2.2* pull-up requirements whether they are muxed or not. Any unused input signals should be pulled to 3.3 V through an 8.2 k $\Omega$   $\pm$  5% resistor to keep them from floating.

### 8.2.6.7 Hot Plug Muxed Signals in Dual Slot Parallel Mode

The Hot Plug signals that connect to the controller are as follows:

**Table 8-12. Dual Slot Parallel Mode Hot Plug Signals Table**

Signal	Type	Muxed Intel® P64H2 Pin				Note
		Bus A	Ball #	Bus B	Ball #	
HxSWITCHA	I	PA_IRQ[15]	F4	PB_IRQ[15]	F1	
HxFAULTA#	I	PA_IRQ[14]	E4	PB_IRQ[14]	E1	
HxPRSNT2A#	I	PA_IRQ[13]	F5	PB_IRQ[13]	D1	
HxPRSNT1A#	I	PA_IRQ[12]	E5	PB_IRQ[12]	C1	
HxM66ENA	I/O	PA_IRQ[11]	D5	PB_IRQ[11]	B1	
HxPCIXCAP1A	I	HPA_SLOT[2]	D20	HPB_SLOT[2]	D22	1
HxPCIXCAP2A	I	HPA_SLOT[1]	C20	HPB_SLOT[1]	C23	1
HxRESETA#	O	PA_GNT[5]	E22	PB_GNT[5]	G4	3
HxGNLEDA	O	HPA_SOC	A19	HPB_SOC	A24	3
HxAMLEDA	O	HPA_SOL	D19	HPB_SOL	C22	3
HxBUSENA#	O	HPA_SORR#	A18	HPB_SORR#	A22	3, 4
HxCLKENA#	O	HPA_SIL#	C21	HPB_SIL#	D24	3, 4
HxPWRENA	O	HPA_SOD	B19	HPB_SOD	C24	3
HxSWITCHB	I	PA_IRQ[10]	C5	PB_IRQ[10]	F2	
HxFAULTB#	I	PA_IRQ[9]	B5	PB_IRQ[9]	E2	
HxPRSNT2B#	I	PA_IRQ[8]	A5	PB_IRQ[8]	D2	
HxPRSNT1B#	I	PA_REQ[5]	F24	PB_REQ[5]	G3	
HxM66ENB	I/O	PA_REQ[4]	F21	PB_REQ[4]	H4	
HxPCIXCAP1B	I	PA_REQ[3]	F19	PB_REQ[3]	H2	
HxPCIXCAP2B	I	HPA_SLOT[0]	A20	HPB_SLOT[0]	B2	1
HxRESETB#	O	HPA_SOR#	B18	HPB_SOR#	A21	3
HxGNLEDB	O	HPA_SIC	A23	HPB_SIC	A23	3
HxAMLEDB	O	HPA_SID	B24	HPB_SID	B24	2
HxBUSENB#	O	PA_GNT[4]	F23	PB_GNT[4]	H5	3, 4
HxCLKENB#	O	PA_GNT[3]	F20	PB_GNT[3]	H3	3, 4
HxPWRENB	O	HPA_SOLR	C19	HPB_SOLR	B22	3

**NOTES:**

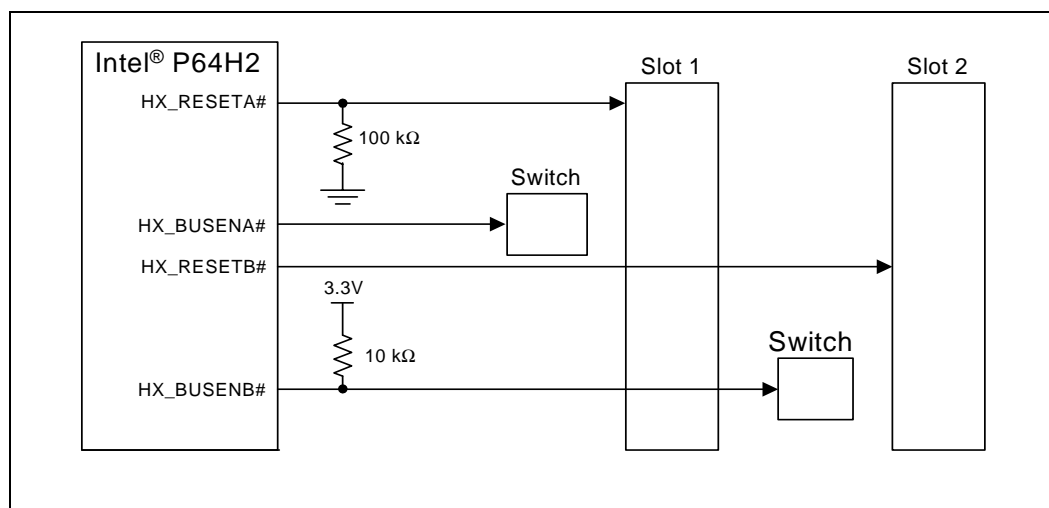
1. HPx\_SLOT [N] are pull-ups/pull-downs. When in dual slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. HPx\_SID must be pulled down on the system board when configuring the P64H2 for dual slot parallel mode so that the LED for slot B on busses A and B remain off during reset.
3. The P64H2 must drive this signal to the corresponding state shown in [Table 8-11](#) in case the system is set up for dual slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the P64H2 in dual slot parallel mode is the same value it would have driven if in serial mode.
4. In parallel mode, the BUSEN# and CLKEN# signals become active low instead of active high, as they are during serial mode.

### 8.2.6.8 SMBus Address Considerations

In Dual Slot Parallel mode, the SMBus address strap pins in Table 8-7 are muxed as Hot Plug control signals HxRESETA# and HxBUSENB#. Therefore, it is recommended that the following technique be used for determining an SMBus address. Pull the PA\_GNT5 (RESETA#) signals to ground through a  $100\text{ k}\Omega \pm 5\%$  resistor. This keeps the reset signal active until the P64H2 is ready for it to become deasserted. Pull the PA\_GNT4 (BUSENB#) signals to 3.3 V through a  $10\text{ k}\Omega \pm 5\%$  resistor. The P64H2 will be able to drive this signal to ground when the signal must be asserted.

Keep in mind that this limits the range of addresses you can achieve. Using this technique, the address is fixed if operating in dual slot mode on both controllers.

**Figure 8-13. Dual Slot Parallel SMBus Circuit**





## 8.2.7 Three or More Slot Serial Mode

Serial Mode allows for three to six slots to be hot pluggable. This mode can also be used to enable slots that are hot pluggable, and others that are not on the same PCI/PCI-X bus.

### 8.2.7.1 Hot Plug and Non-Hot Plug Combinations

To accomplish hot plug and non-hot plug combinations, put the non-hot pluggable devices on their own hot plug serialization logic (for M66EN and PCIXCAP), and scan them in for software to view. Don't electrically isolate those devices—allow software to see their capabilities to choose bus frequency properly.

### 8.2.7.2 Required Additional Logic

Serial Mode requires a power switch to be used to turn the slot power on and off on all Hot Pluggable slots. Serial Mode also requires the use of a bus and clock switch. In addition, Serial Mode requires auto bus and clock disable logic to immediately disable the PCI bus and clock when the power fault signal (from the power switch) goes active.

If the platform supports PME# or SMBus connections to the slots, isolation logic is required to disconnect these signals before inserting or removing a card. See the *PCI Hot Plug Specification, Revision 1.1* for implementation details.

### 8.2.7.3 Debounced Hot Plug Switch Input

The switch inputs to the serialization/deserialization logic may require debouncing logic. This depends upon the logic used for serialization, and is left up to the individual designer.

### 8.2.7.4 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification, Revision 2.2* for this circuit. An example of this circuit is also contained in the reference schematics.

### 8.2.7.5 HPxSLOT [2:0]

The HPxSLOT [2:0] pins are pull-ups/pull-downs that are used to determine the slot count and mode of operation for the P64H2 Hot Plug Controller. These pins should be strapped to the proper slot count value. See [Table 8-8](#).

### 8.2.7.6 Stutter Logic for Implementing Fewer Than Six Slots

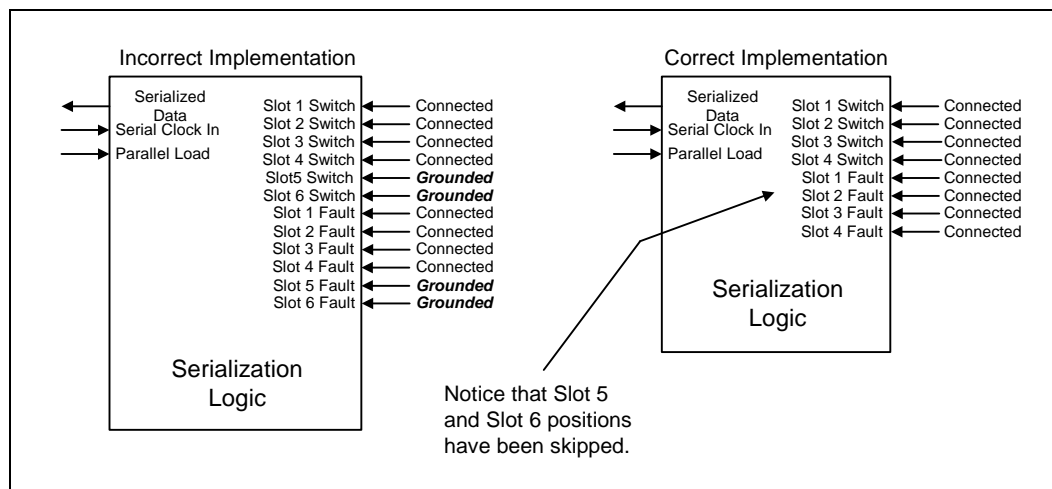
The serialized input/output data stream effectively stutters around the unused bit positions corresponding with the number of Hot Plug slots determined by HPx\_SLOT[2:0]. This reduces the amount of logic required to implement fewer than six slots. If HPx\_SLOT[2:0] is strapped to enable four Hot Pluggable slots, bit positions 4 and 5 would be skipped. Refer to [Figure 8-15](#) for an example of this. Note that this concept also applies to the output data stream as well.



Table 8-13. Shift Register Input Data

Bit	Byte 0	Byte 1	Byte 2	Byte 3
0	Slot 1 switch (0 = closed)	Slot 1 fault# (0 = fault)	Slot 1 present bit 2	Slot 1 present bit 1
1	Slot 2 switch	Slot 2 fault#	Slot 2 present bit 2	Slot 2 present bit 1
2	Slot 3 switch	Slot 3 fault#	Slot 3 present bit 2	Slot 3 present bit 1
3	Slot 4 switch	Slot 4 fault#	Slot 4 present bit 2	Slot 4 present bit 1
4	Slot 5 switch	Slot 5 fault#	Slot 5 present bit 2	Slot 5 present bit 1
5	Slot 6 switch	Slot 6 fault#	Slot 6 present bit 2	Slot 6 present bit 1
6	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
7	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
Bit	Byte 4	Byte 5	Byte 6	Byte 7
0	Slot 1 M66EN	Slot 1 PCIXCAP1	Slot 1 PCIXCAP2	User Defined
1	Slot 2 M66EN	Slot 2 PCIXCAP1	Slot 2 PCIXCAP2	User Defined
2	Slot 3 M66EN	Slot 3 PCIXCAP1	Slot 3 PCIXCAP2	User Defined
3	Slot 4 M66EN	Slot 4 PCIXCAP1	Slot 4 PCIXCAP2	User Defined
4	Slot 5 M66EN	Slot 5 PCIXCAP1	Slot 5 PCIXCAP2	User Defined
5	Slot 6 M66EN	Slot 6 PCIXCAP1	Slot 6 PCIXCAP2	User Defined
6	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
7	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)

Figure 8-15. Four Slot Stutter Logic Implementation Example



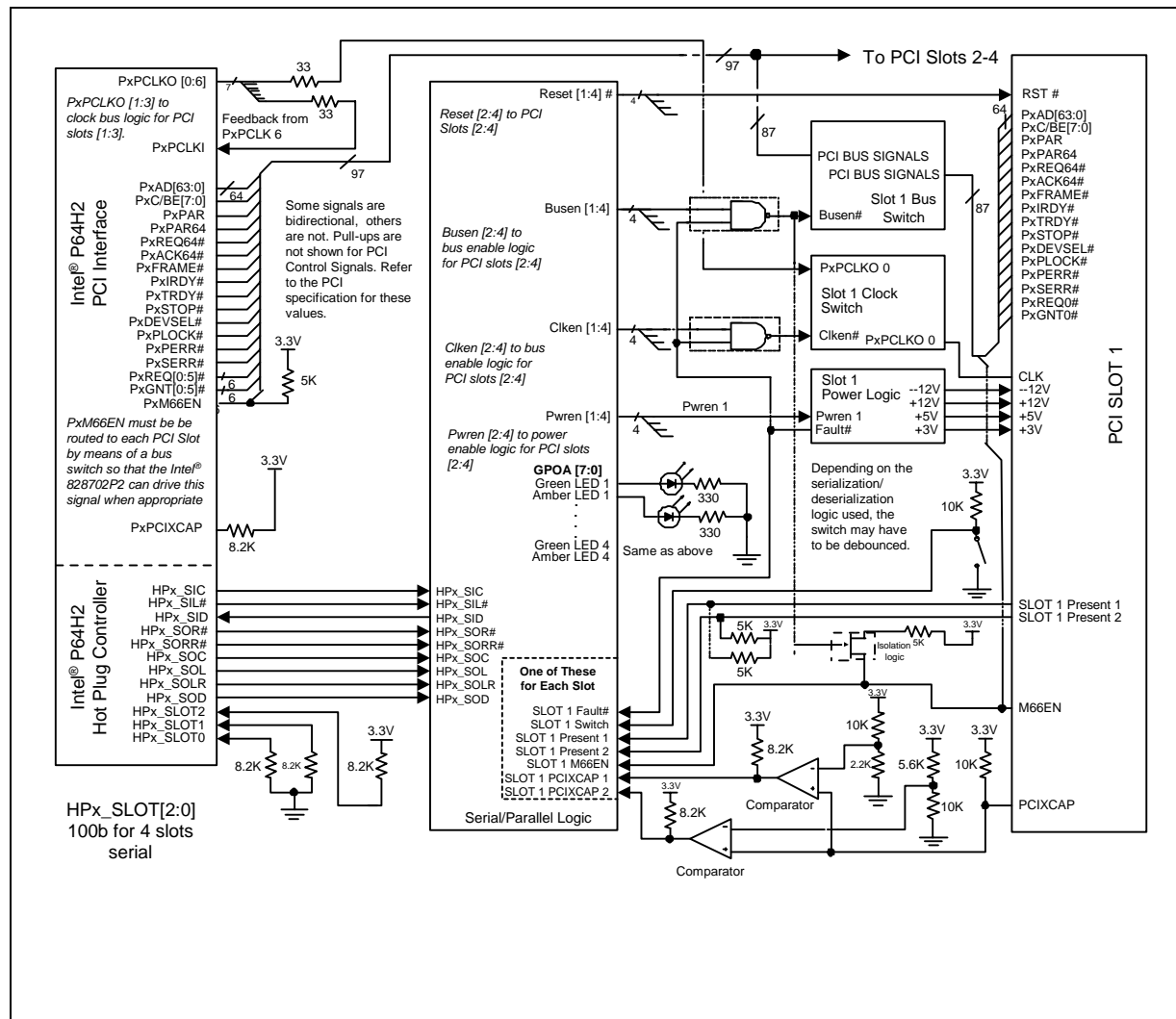
### 8.2.7.7 Pull-Ups/Pull-Downs in Three or More Slot Serial Mode

All PCI signals should follow the *PCI Local Bus Specification, Revision 2.2* pull-up requirements whether they are muxed or not. Any unused input signals should be pulled to 3.3 V through an  $8.2\text{ k}\Omega \pm 5\%$  resistor to keep them from floating.

### 8.2.7.8 Reference Schematic for Serial Mode

The following schematic is based on definition and simulation of the P64H2. This schematic has not been fully validated.

Figure 8-16. Reference Schematic for Serial Mode



## 8.2.8 Intel® P64H2 PCI Interface PCIXCAP and M66EN Pins

### 8.2.8.1 PCIXCAP Pin Requirements

During all modes of the P64H2 Hot Plug Controller operation, the P64H2 PCI/PCI-X interface pin PxPCIXCAP is not used. This pin should be tied to either 3.3 VCC or ground through an 8.2 k $\Omega$  resistor to avoid having this line float.

The slot-specific HxPCIXCAP1 and HxPCIXCAP2 pins should be connected to their associated slot. See [Section 8.2.5](#), [Section 8.2.6](#), and [Section 8.2.6.9](#) for more information on properly decoding PCI/PCI-X capability.

### 8.2.8.2 M66EN Pin Requirements

When operating in Single Slot Parallel Mode, the P64H2 never drives PxM66EN. This pin should be tied to either 3.3 VCC or ground through an 8.2 k $\Omega \pm 5\%$  resistor to avoid having this line float. M66EN on the slot must be connected to the associated HxM66EN pin with a pull-up/pull-down on the motherboard. If the slot is to be a 33 MHz slot, then M66EN must be pulled to ground on the motherboard. This will make the slot a 33 MHz PCI slot always. If the M66EN pin is pulled high, then the slot cannot be run at 33 MHz PCI. This means that after a card is powered up at 33 MHz (hot plug default), software must reset the bus to at least 66 MHz PCI mode (or a PCI-X mode) before any software attempts accesses to the PCI card. Otherwise, the card could experience operational problems if it requires M66EN for setting up PLLs, etc.

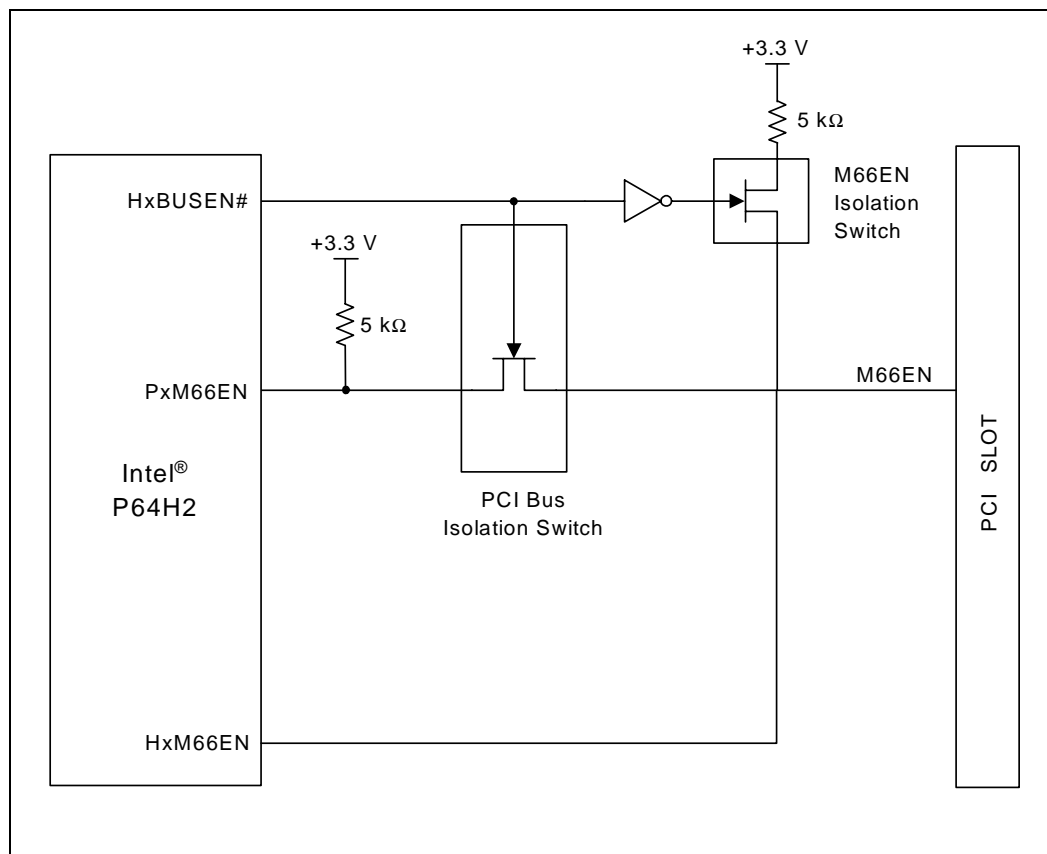
In Dual Slot Parallel and Serial Modes, the PxM66EN pin (on the P64H2 PCI/PCI-X interface) is a switched PCI bus signal that must be tied to all the slots through isolation logic. All cards must be able to see the value of PxM66EN being driven by the P64H2 when coming out of reset. The HxM66EN pins (on the P64H2 Hot Plug Interface) should be connected to their associated slots.

The PxM66EN and HxM66EN pins each require 5 k $\Omega \pm 5\%$  pull-up resistors as specified in *PCI Local Bus Specification, Revision 2.2*. When the slot is connected to the bus, the P64H2 will be sinking through both resistors, which is a violation of specification. The following sections describe two possible M66EN design solutions.

## M66EN Isolation Switch Solution

One possible solution is to place a single  $5\text{ k}\Omega \pm 5\%$  pull-up on the P64H2 side of the isolation logic and a  $5\text{ k}\Omega \pm 5\%$  pull-up on the slot side after the isolation logic, but with its own isolation switch, which uses an inverted version of the bus enable control signal. This way, when the isolation logic has the bus disconnected, the slot side will be pulled up with a  $5\text{ k}\Omega \pm 5\%$  resistor. When the isolation logic has the bus connected, the slot side resistor will be isolated, and the M66EN line will be pulled up by the  $5\text{ k}\Omega \pm 5\%$  pull-up on the P64H2 side of the isolation logic. Using this method, the P64H2 would only be sinking through a single  $5\text{ k}\Omega$  resistor at any time and would always be meeting the *PCI Local Bus Specification, Revision 2.2* on the M66EN pull-up (*PCI Local Bus Specification, Revision 2.2, Section 7.7.7*). See [Figure 8-17](#).

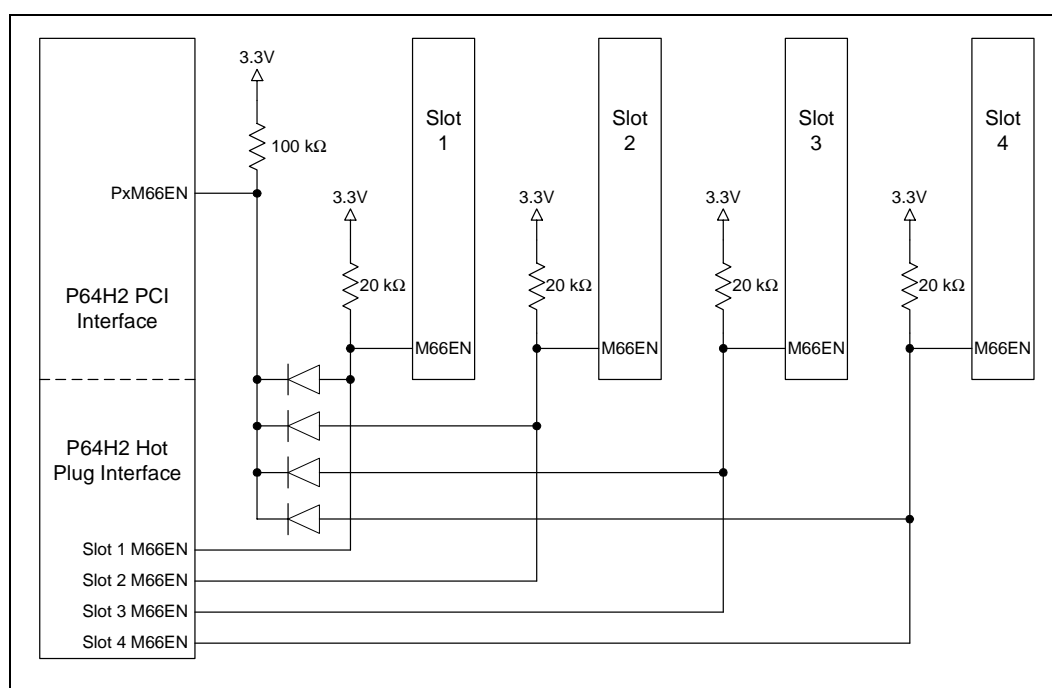
**Figure 8-17. M66EN Isolation Switch Solution**



## M66EN Diode Solution

Another possible solution is to use diodes to isolate the individual slots from one another while still allowing the P64H2 to drive the M66EN signals to ground. The P64H2 PCI interface PxM66EN signal should be pulled up to 3.3 V through a  $100\text{ k}\Omega \pm 5\%$  resistor. This signal would then be connected to the individual slots through a reverse biased diode (one diode per slot). The PCI slots should also be pulled up individually to 3.3 V through a resistor of value such that the equivalent of all the resistances on the M66EN bus is approximately  $5\text{ k}\Omega$  (the PCI recommended value). This circuit will allow the P64H2 to pull the slots' M66EN to ground during initial power-up. During normal operation, each of the slots' M66EN signals will be isolated from one another allowing for polling of the Hot Plug HxM66EN input for slot capability. Figure 8-18 shows the diode solution implemented in Serial Mode, where "Slot x M66EN" is a serialized input to the Hot Plug Controller.

Figure 8-18. M66EN Diode Solution



**NOTE:** All PCI signals, muxed or not, must follow PCI Specification 2.2 pull-up requirements.

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# I/O Controller Hub

# 9

## 9.1 IDE Interface

This section contains guidelines for connecting and routing the ICH3-S IDE interface. The ICH3-S has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH3-S has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0  $\Omega$  resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5 mil traces on 7 mil spaces, and must be less than 8 inches long (from ICH3-S to IDE connector). Additionally, maximum length difference between the longest and shortest trace lengths of a channel is 0.5 inch.

### 9.1.1 Cabling

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** The capacitance of each IDE cable must be less than 35 pF.
- **Placement:** A maximum of 6 inches is allowed between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (no more than 6 inches away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH3-S Placement:** The ICH3-S must be placed equal to or less than 8 inches from the ATA connector(s).

## 9.1.2 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH3-S IDE Controller supports PIO, Multi-word (8237 style) DMA and Ultra DMA modes 0 through 5. The ICH3-S must determine the type of cable that is present to configure itself for the fastest possible transfer mode the hardware can support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than 2 (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, and so on. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification can be obtained from the Small Form Factor Committee.

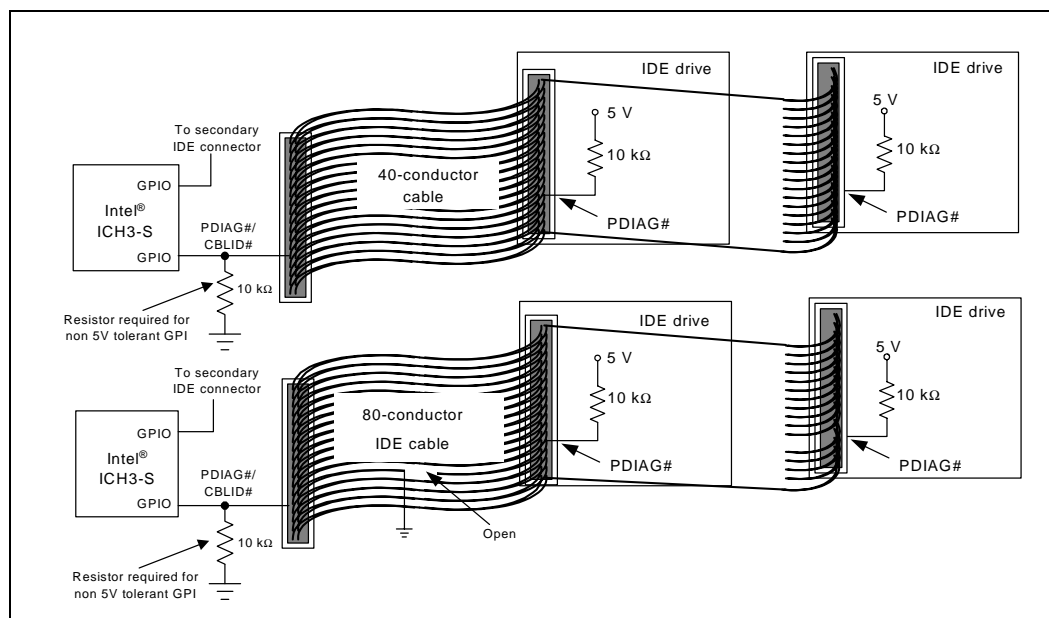
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH3-S requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism.

### 9.1.2.1 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in [Figure 9-1](#). All IDE devices have a 10 k $\Omega$  pull-up resistor to 5 V on this signal. Not all of the GPI and GPIO pins on the ICH3-S are 5 V tolerant. A 10 k $\Omega$   $\pm$  5% pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present. The pull-down resistor also allows for the use of a non-5 V tolerant GPIO.

**Figure 9-1. Combination Host-Side/Device-Side IDE Cable Detection**





This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, then a 40-conductor cable is present in the system and Ultra DMA modes greater than Mode 2 (Ultra ATA/33) must not be enabled.

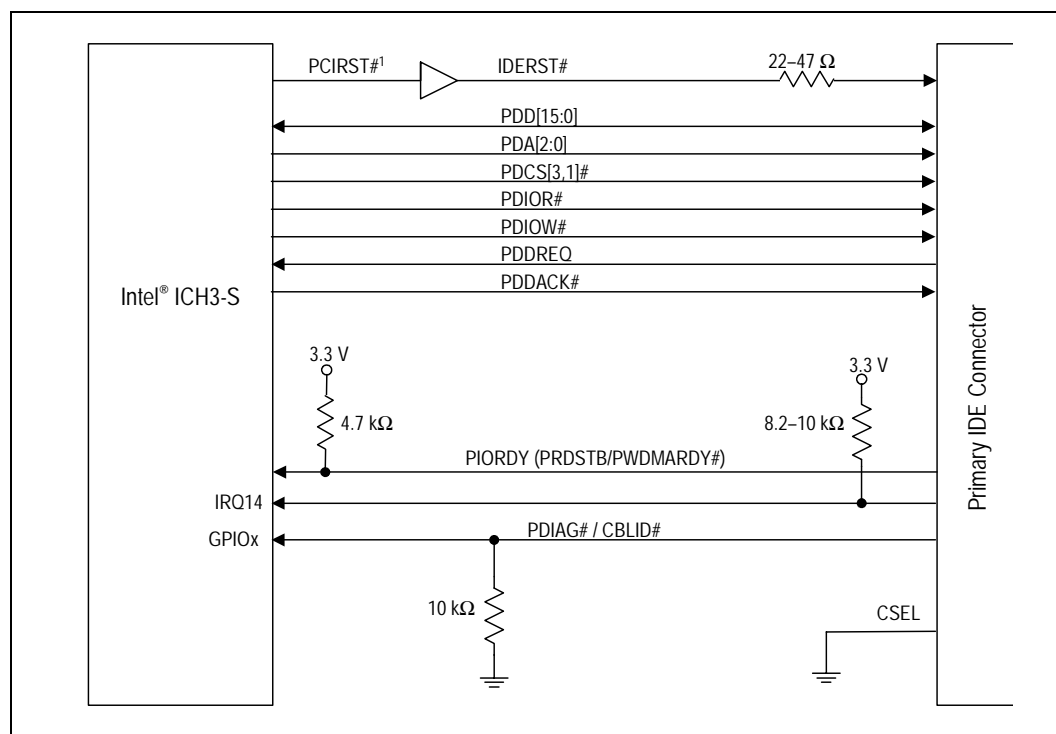
If PDIAG#/CBLID# is detected low, then an 80-conductor cable may be in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a “1,” then an 80-conductor cable is present. If this bit is “0” then a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and notify the user of the problem.

### 9.1.3 Primary IDE Connector Requirements

The requirements for the primary IDE connector are shown in Figure 9-2.

- A 22  $\Omega$  to 47  $\Omega$  series resistor is required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 k $\Omega$  to 10 k $\Omega$  pull-up resistor is required on IRQ14 to VCC\_3.3.
- A 4.7 k $\Omega \pm 5\%$  pull-up resistor to VCC\_3.3 is required on PIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 k $\Omega \pm 5\%$  resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPIOx pin from floating if a device is not present on the IDE interface.

Figure 9-2. Connection Requirements for Primary IDE Connector



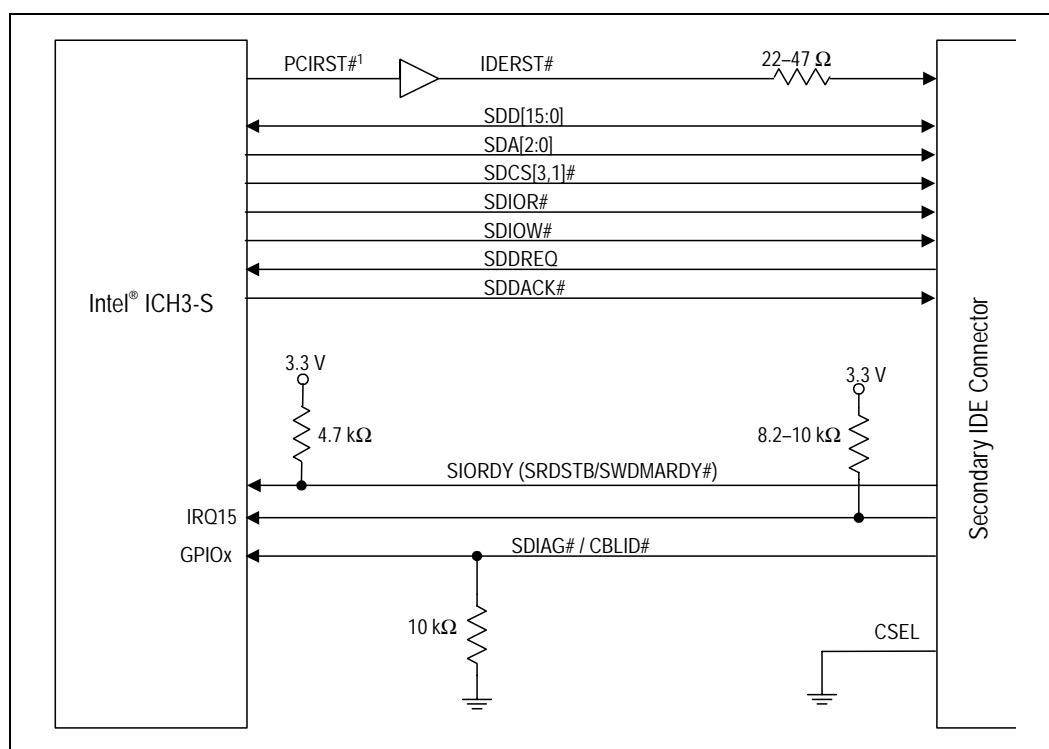
**NOTE:** <sup>1</sup>Because of ringing, PCIRST# must be buffered.

### 9.1.4 Secondary IDE Connector Requirements

The requirements for the secondary IDE connector are shown in Figure 9-3.

- 22  $\Omega$  – 47  $\Omega$  series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 k $\Omega$  to 10 k $\Omega$  pull-up resistor is required on IRQ15 to VCC\_3.3.
- A 4.7 k $\Omega \pm 5\%$  pull-up resistor to VCC\_3.3 is required on SIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 k $\Omega$  resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPIOx pin from floating if a device is not present on the IDE interface.

Figure 9-3. Connection Requirements for Secondary IDE Connector

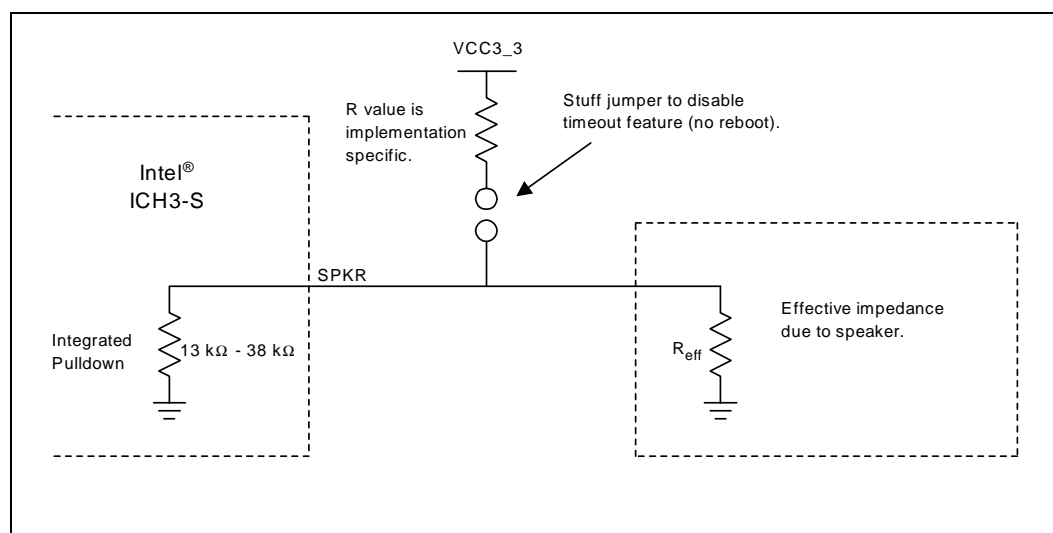


**NOTE:** <sup>1</sup>Because of ringing, PCIRST# must be buffered.

## 9.2 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the “TCO Timer Reboot function” based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH3-S sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO\_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable TCO timer reboot, a jumper can be populated to pull the signal line high (see Figure 9-4). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (REFF), and the ICH3-S’s integrated pull-down resistor will be read as logic high ( $0.5 V_{CC\_3.3}$  to  $V_{CC\_3.3} + 0.5 V$ ).

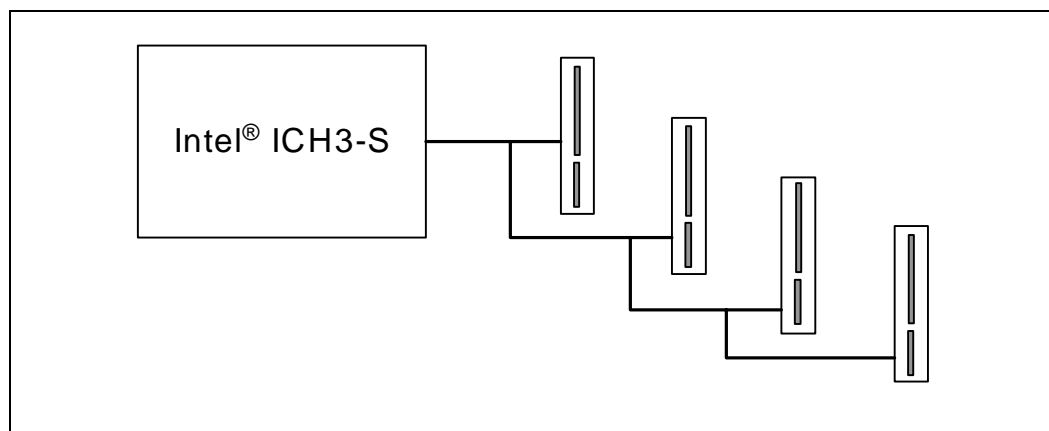
Figure 9-4. Example Speaker Circuit



## 9.3 PCI

The ICH3-S provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH3-S is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH3-S supports six PCI Bus masters (excluding the ICH3-S), by providing six REQ# / GNT# pairs. In addition, the ICH3-S supports two PC/PCI REQ# / GNT# pairs, one of which is multiplexed with a PCI REQ# / GNT# pair.

**Figure 9-5. PCI Bus Layout Example**

## 9.4 USB

The ICH3-S contains three UHCI Host Controllers. Each UHCI Controller includes a root hub with two separate USB ports, for a total of six USB ports. This section provides guidelines for routing USB.

### 9.4.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems. USB validation efforts have focused on a ground referenced design.

1. Place the ICH3-S and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB signals should be ground referenced (on layers 3 and 6).
3. Route USB signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90 degrees, use two 45 degree turns or an arc instead of a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on USB signals should be avoided because stubs have an effect on signal quality. If stubs are necessary, none should be greater than 200 mils.
7. Route all traces over continuous ground planes with no interruptions. Avoid crossing over anti-etch if possible; this increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.
8. Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, and can be very difficult to filter out.

9. Keep traces at least 50 mils away from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.

## 9.4.2 USB Trace Separation

Use the following separation guidelines.

- Recommended trace width and separation is 5 mil trace width with 6 mil spacing (90  $\Omega$  differential impedance).
- Maintain parallelism between USB differential signals, with the trace spacing needed to achieve 90  $\Omega$  differential impedance.
- Use at a minimum 20 mil spacing between USB signal pair and other traces on the PCB. This helps to prevent crosstalk. If possible, keep clock and PCI traces at least 50 mils from the USB differential pairs.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk.

## 9.4.3 USB Trace Length Matching

Trace length match USB signal pair traces. The maximum trace length mismatch between USB signal pair should be no greater than 150 mils.

## 9.4.4 Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits, voids, and cut-outs.

### 9.4.4.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane:

- Traces should not cross anti-etch because it greatly increases the return path for those signal traces. This is true of all USB signals, high-speed clocks, and signal traces, as well as slower signal traces that might be coupling to them.
- Avoid routing USB signals within 50 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

### 9.4.4.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guideline for the GND plane:

- Void anti-etch on the GND plane.

## 9.4.5 EMI Considerations

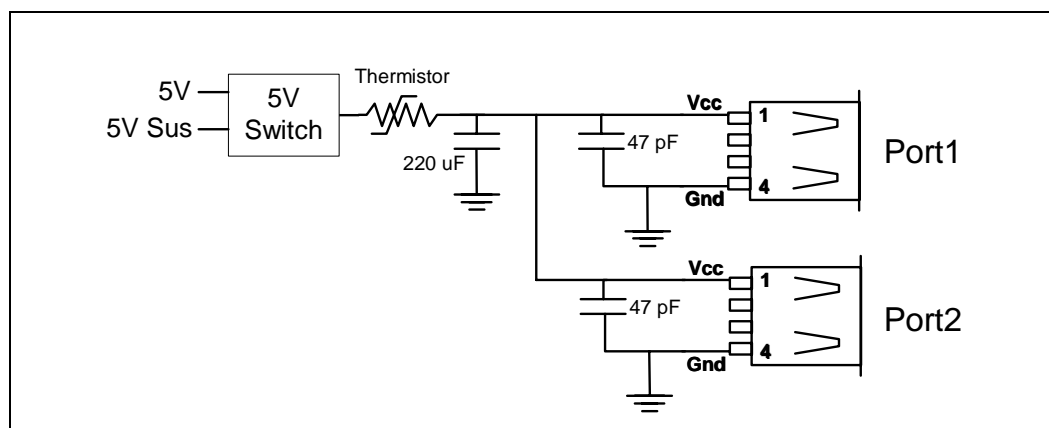
An optional 47 pF capacitor may be placed as close to the USB connector as possible on the USB data lines. This capacitor can be used for improved signal quality (rise/fall time), and to help minimize EMI radiation.

**Note:** Any EMI or ESD solution should be placed as close to the port as possible. For example, if using a front-panel daughtercard, the EMI/ESD solution should be placed on the daughtercard.

## 9.4.6 USB Power Line Layout Topologies

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably a plane.

**Figure 9-6. Suggested USB Downstream Power Connection**



## 9.5 Intel® ICH3-S SMBus/SMLink Interface

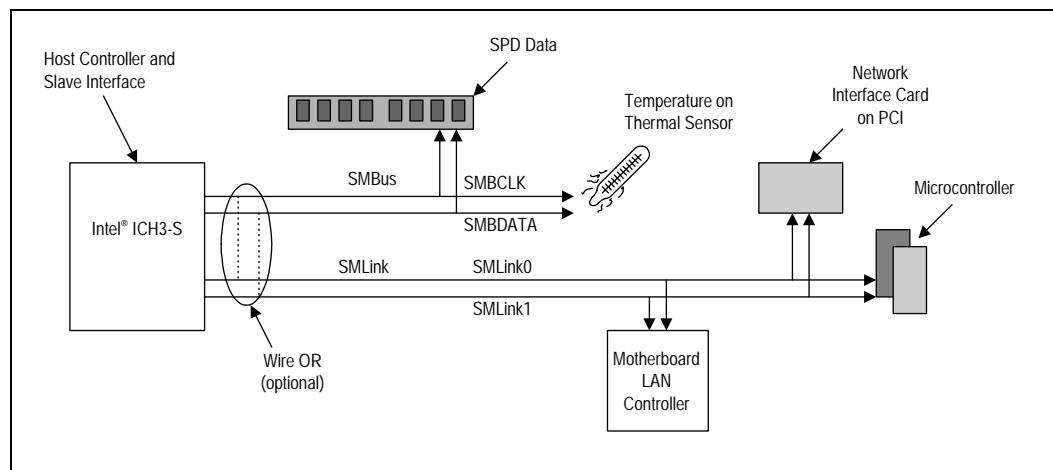
The SMBus interface on the ICH3-S uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH3-S. If the SMBus is used only for the SPD EEPROMs (one on each DIMM), both signals should be pulled up with a  $4.7\text{ k}\Omega \pm 5\%$  resistor to VCC\_3.3.

The ICH3-S incorporates an SMLink interface supporting Alert on LAN\*, Alert on LAN2\*, and a slave functionality. This interface uses two signals, SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal, and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMBus Slave Interface.

For Alert on LAN functionality, the ICH3-S transmits heartbeat and event messages over the interface. When using the 82562EM Platform LAN Connect Component, the ICH3-S's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2-enabled LAN Controller (i.e., Intel® 82550) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH3-S SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.1 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (such as 82550) to access targets on the SMBus as well as the ICH3-S Slave interface. Additionally, the ICH3-S supports slave functionality, including the Host Notify protocol, on the SMLink pins. This is done by connecting SMLink0 to SMBCLK and SMLink1 to SMBDATA.

**Figure 9-7. Intel® ICH3-S SMBus / SMLink Interface**



Intel does not support external access of the ICH3-S's Integrated LAN Controller via the SMLink interface. In addition, Intel does not support access of the ICH3-S's SMBus Slave Interface by the ICH3-S's SMBus Host Controller. Refer to the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

## 9.5.1 SMBus Design Considerations

Designing an SMBus using the ICH3-S is based on the power supply source for the SMBus microcontrollers. For the platform, all devices are powered by VCC\_3.3; therefore, the preferred design choice is the unified VCC\_3.3 architecture.

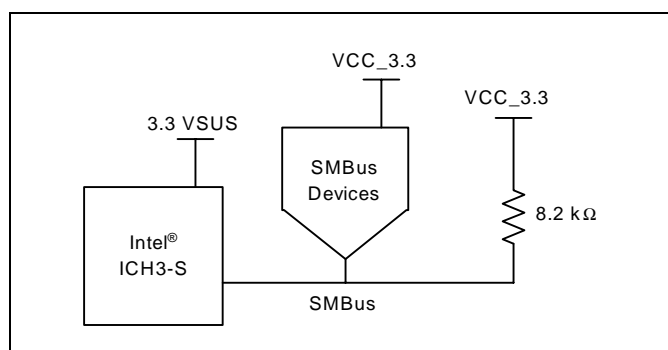
## 9.5.2 General Design Note

The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is  $8.2\text{ k}\Omega \pm 5\%$ . This should prevent the SMBus signals from floating, which could cause leakage in the ICH3-S and other devices.

## 9.5.3 The Unified VCC\_CORE Architecture

In the unified VCC\_CORE architecture, all SMBus devices are powered by the VCC\_3.3 supply. This architecture in [Figure 9-8](#) allows none of the devices to operate in STR, minimizing the load on 3.3 V SUSPEND.

Figure 9-8. Unified VCC\_3.3 Architecture

**NOTES:**

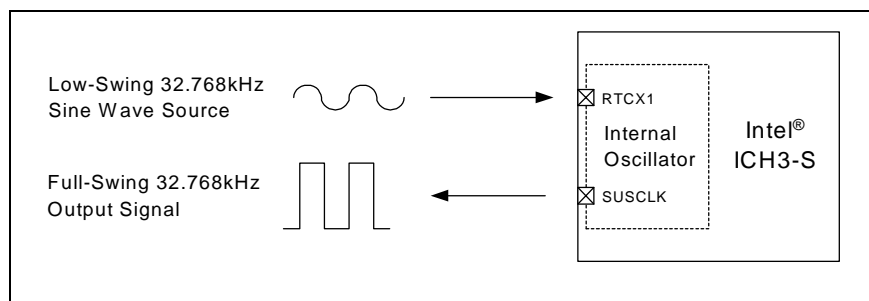
1. The SMBus device must be back-drive safe while its supply (VCC\_3.3) is off and 3.3 V SUS is still powered.
2. In suspended modes where VCC\_3.3 is OFF and 3.3 V SUS is on, the VCC\_3.3 node will be very near ground. In this case, the input leakage of the ICH3-S will be approximately 10  $\mu$ A.

## 9.6 Real Time Clock (RTC)

The ICH3-S contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down.

The ICH3-S uses a crystal circuit that generates a low-swing 32 kHz input sine wave. The RTCX1 input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH3-S, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use illustrated in Figure 9-9. This ICH3-S output ball is called SUSCLK.

Figure 9-9. RTCX1 and SUSCLK Relationship



For further information on the RTC, consult Intel application note *AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions* (<http://developer.intel.com/design/chipsets/aplnots/292276.htm>).

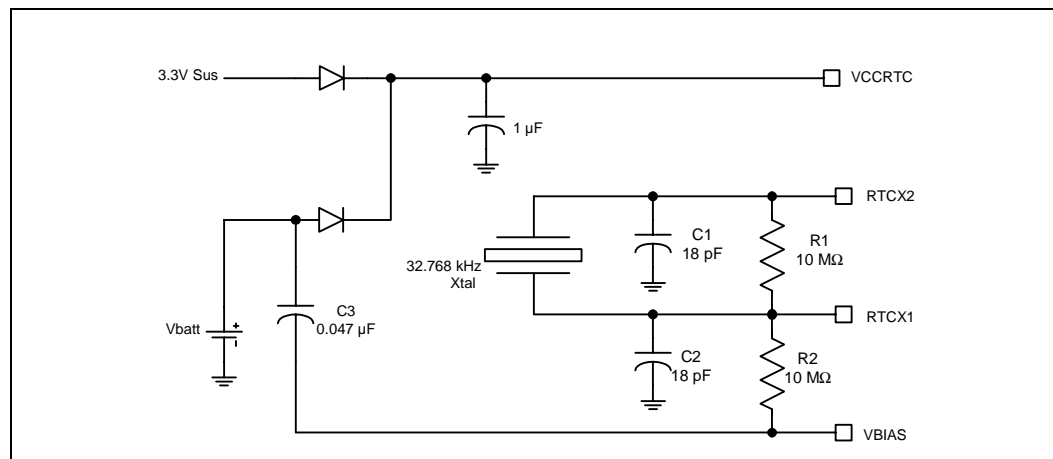
This section presents the recommended hookup for the RTC circuit for the ICH3-S.



## 9.6.1 RTC External Circuit

The ICH3-S RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 9-10 documents the external circuitry that comprises the oscillator of the ICH3-S RTC.

Figure 9-10. RTC External Circuitry

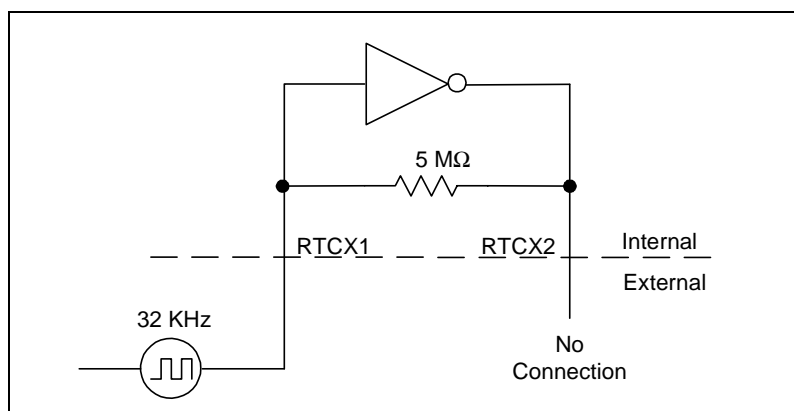


### NOTES:

1. The exact capacitor values must be based on the crystal maker recommendation. (Typical values for C1 and C2 are 18 pF for a crystal load of 12 pF.)
2. VCCRTC: Power for RTC Well
3. RTCX2: Feedback for the external crystal
4. RTCX1: Input to the internal oscillator
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.

**Note:** Even if the ICH3-S internal RTC is not used, it is still necessary to supply clock inputs to RTCX1 and RTCX2 pins of the ICH3-S because other signals are gated with that clock in suspend modes. However, in this case the frequency (32.768 kHz) of the clock inputs is not critical. A lower-cost crystal can be used, or a single clock input can be driven into the RTCX1 pin with the RTCX2 pin left as no connect; Figure 9-11 illustrates this. This is not a validated configuration with ICH3-S.

Figure 9-11. RTC Connection When Not Using Internal RTC



## 9.6.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C3 must be 0.047  $\mu$ F, and capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C1 + C_{in1} + C_{trace1}) * (C2 + C_{in2} + C_{trace2})] / [(C1 + C_{in1} + C_{trace1} + C2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

Cload = Crystal's load capacitance. This value can be obtained from crystal's specification.

Cin1, Cin2 = input capacitances at RTCX1, RTCX2 balls of the ICH3-S. These values can be obtained in the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*.

Ctrace1, Ctrace2 = Trace length capacitances measured from crystal terminals to the RTCX1 and RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces, and the length of the traces. Typical value is approximately:

$$C_{trace} = \text{trace length} * 2 \text{ pF / inch (dependent upon board characteristics)}$$

Cparasitic = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates, and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C1 and C2 can be chosen such that C1 = C2. Using the equation of Cload above, the value of C1 and C2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C2 can be chosen such that C2 > C1. Then C1 can be trimmed to obtain 32.768 kHz.

In certain conditions, both C1 and C2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1 and C2 values are smaller than the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of the practical values C1, C2 in the case that theoretical values can not guarantee the accuracy of the RTC in a low temperature condition:

### Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH3-S, the calculated values of C1 = C2 are 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C, the frequency stability of the crystal gives -23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C1 and C2 are chosen to be 6.8 pF instead of 10 pF. This will make the RTC oscillate at a higher frequency at room temperature (+23 ppm), but this configuration of C1 / C2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and C2 is the **practical value**.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree squared). The effect of the changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

### 9.6.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH3-S requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Route the RTC circuit short to simplify the trace length measurement and increase accuracy when calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Reduce trace signal coupling by avoiding routing of adjacent PCI signals close to RTCX1, RTCX2, and VBIAS.
- A ground guard plane is highly recommended.

### 9.6.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH3-S is not powered by the system.

Example batteries are: Duracell® 2032, 2025, or 2016 (or equivalent), which can give many years of operation.

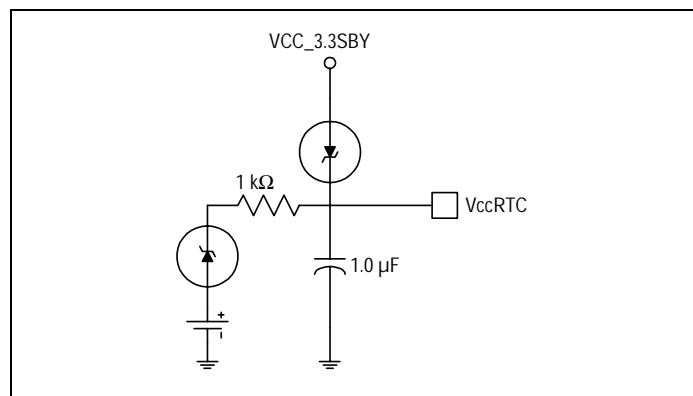
Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable), and the average current required is 3 µA, the battery life will be at least:

$$170,000 \mu\text{Ah} / 3 \mu\text{A} = 56,666 \text{ h} = 6.4 \text{ years}$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. The battery voltage of the RTC must be greater than 2 V at all times to ensure the accuracy of the RTC clock.

Connect the battery to the ICH3-S via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH3-S RTC-well to be powered by the battery when the system power is not available, and by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. [Figure 9-12](#) is an example of a diode circuit.

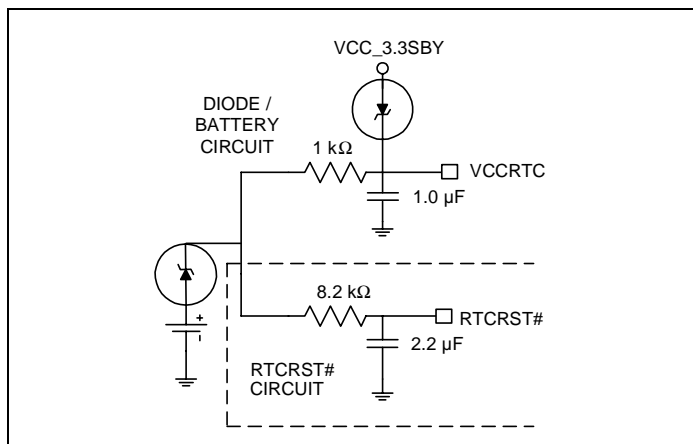
**Figure 9-12. A Diode Circuit to Connect RTC External Battery**



As noted, a standby power supply should be used in a server system to provide continuous power to the RTC when available to significantly increase the RTC battery life.

## 9.6.5 RTC External RTCRST# Circuit

Figure 9-13. RTCRST# External Circuit



The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10 ms – 20 ms. When RTCRST# is asserted, bit 2 (RTC\_PWR\_STS) in the GEN\_PMCN\_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. Because of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in [Figure 9-12](#)) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. [Figure 9-13](#) is an example of RTCRST# circuitry that is used in conjunction with the external diode circuit.

## 9.6.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see [Figure 9-10](#)); therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 filters out most of the AC signals that exist on this ball. However, the noise on this ball should be kept to a minimum to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1 and RTCX2 signals (using Op-Amp). See application note *AP-728, Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*, for further details on measuring techniques.

**Note:** VBIAS is also very sensitive to environmental conditions.

### 9.6.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30% and 70%.

If the SUSCLK duty cycle is beyond the 30%–70% range, there is a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using a normal probe (50  $\Omega$  input impedance probe), and it is an appropriate signal to check the RTC frequency to determine the accuracy of the ICH3-S RTC clock.

### 9.6.8 RTC-Well Input Strap Requirements

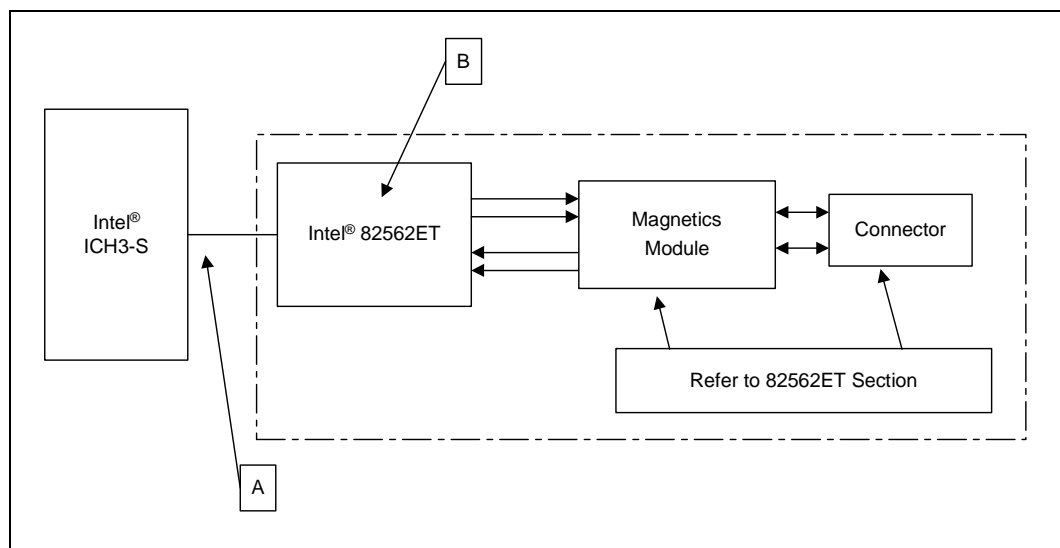
All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in [Figure 9-13](#), meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

## 9.7 Internal LAN Layout Guidelines

The ICH3-S provides various options for integrated LAN capability. The platform supports several components depending on the target market. The guidelines use the term 82562ET to refer to both the 82562ET, and the 82562EM. The 82562EM is specified in those cases where a difference exists.

Platform LAN Connect Component	Connection	Features
82562EM	Advanced 10/100 Ethernet	Alert on LAN* & Ethernet 10/100 Connection
82562ET	10/100 Ethernet	Ethernet 10/100 Connection

Design guidelines are provided for each required interface and connection. Refer to [Figure 9-14](#) and [Table 9-1](#) for the corresponding section of the design guide.

**Figure 9-14. Platform LAN Connect****Table 9-1. LAN Design Guide Section Reference**

Layout Section	Figure 9-14 Reference	Design Guide Section
ICH3-S – LAN Connect Interface	A	<a href="#">Section 9.7.1, Intel® ICH3-S – LCI (LAN Connect Interface) Guidelines</a>
General Routing Guidelines	B	<a href="#">Section 9.7.2, General LAN Routing Guidelines and Consideration</a>
82562ET / 82562EM	B	<a href="#">Section 9.7.3, Intel® 82562ET/EM Guidelines</a>

## 9.7.1 LCI (LAN Connect Interface) Guidelines

This section contains guidelines on how to implement a PLC (Platform LAN Connect) device on a system motherboard using LCI. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN\_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH3-S to LAN component interface. The following signal lines are used on this interface:

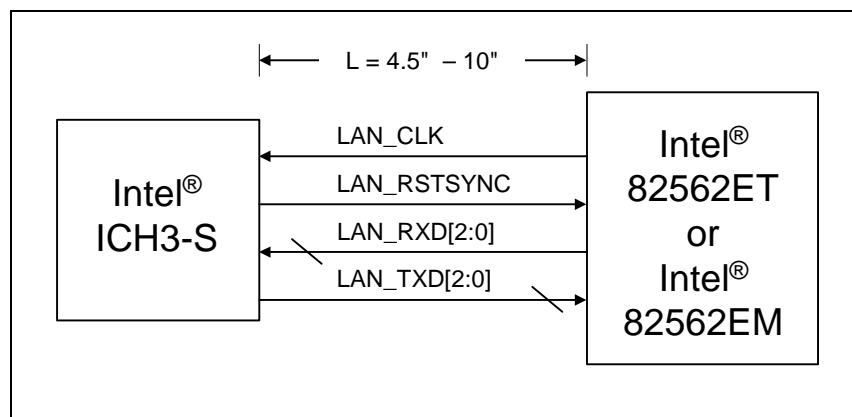
- LAN\_CLK
- LAN\_RSTSYNC
- LAN\_RXD[2:0]
- LAN\_TXD[2:0]

This interface supports 82562ET/82562EM components. Signal lines LAN\_CLK, LAN\_RSTSYNC, LAN\_RXD[0], and LAN\_TXD[0] are shared by all components.

### 9.7.1.1 Bus Topology

The LAN Connect Interface must be configured in direct point-to-point connection between the ICH3-S and the LAN component topology. (Refer to [Figure 9-15](#).)

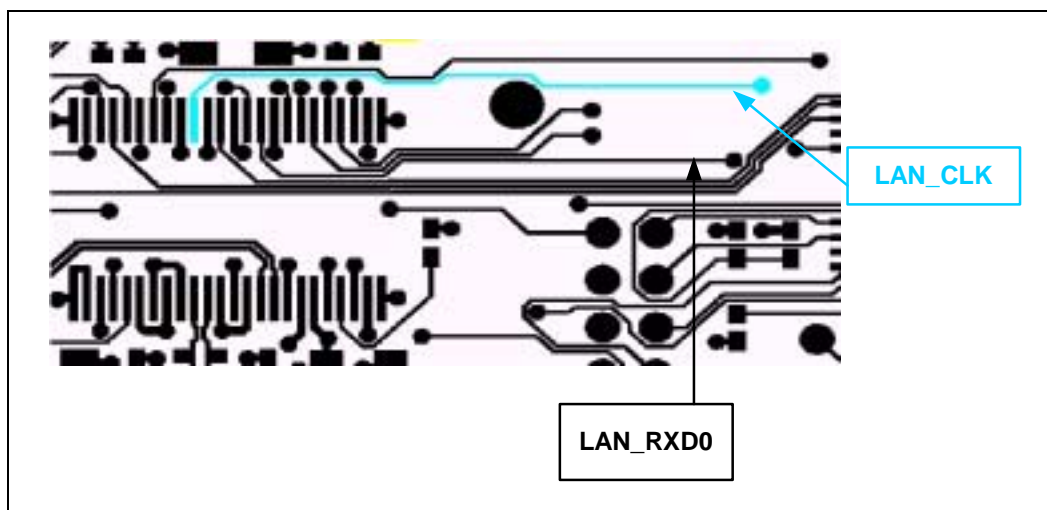
**Figure 9-15. Point-to-Point Interconnect Guideline**



### 9.7.1.2 Signal Routing and Layout

Route the LCI signals carefully on the motherboard to meet the timing and signal quality requirements of this interface specification. The board designer should simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard, the length of each data trace should be either equal in length to the LAN\_CLK trace, or up to 0.5" shorter than the LAN\_CLK trace. (LAN\_CLK should always be the longest motherboard trace in each group.)

Figure 9-16. LAN\_CLK Routing Example



### 9.7.1.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. tRMATCH is the sum of the trace length mismatch between LAN\_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace must be either equal to or up to 0.5 inch shorter than the LAN\_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-LCI signals.

### 9.7.1.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of  $60\ \Omega \pm 15\%$  is strongly recommended; otherwise, signal integrity requirements may be violated.

### 9.7.1.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A  $33\ \Omega$  series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.



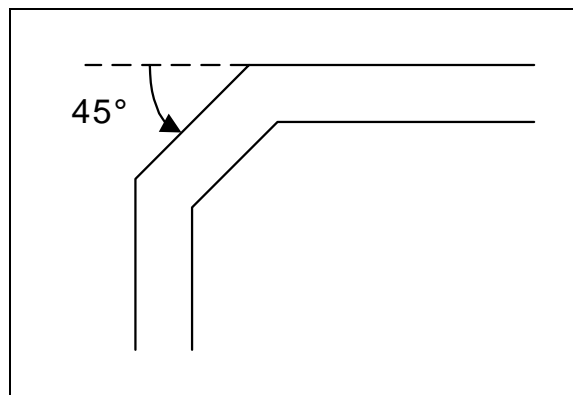
## 9.7.2 General LAN Routing Guidelines and Considerations

### 9.7.2.1 General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER [Bit Error Rate].)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces, or closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 degree bends instead. Refer to [Figure 9-17](#).
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

**Figure 9-17. Routing a 90 Degree Bend**



### 9.7.2.2 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be  $\sim 100\ \Omega$ . It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to  $10\ \Omega$ , when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetic edge of the board.

### 9.7.2.3 Signal Isolation

Follow these rules for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

### 9.7.2.4 Power and Ground Connections

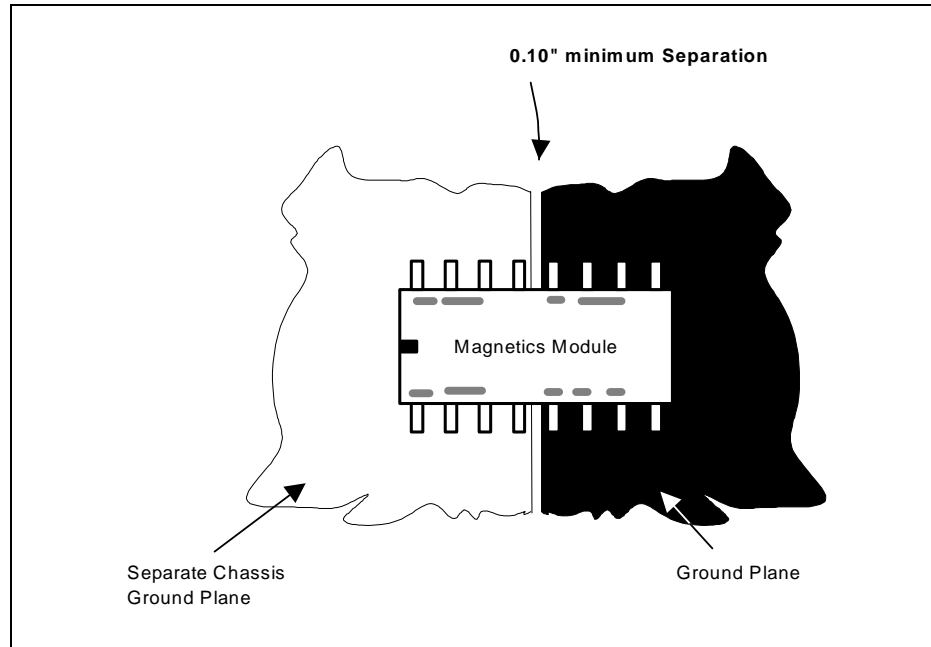
Follow these rules for power and ground connections:

- All VCC balls should be connected to the same power supply.
- All VSS balls should be connected to the same ground plane.
- Four to six decoupling capacitors, including two  $4.7\ \mu\text{F}$  capacitors, are recommended.
- Place decoupling as close as possible to power balls.

### 9.7.2.5 General Power and Ground Plane Consideration

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

**Figure 9-18. Ground Plane Separation**



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. These will significantly reduce EMI radiation.

The following are guidelines that help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a plane split). If vacant areas exist on a ground or power plane, avoid routing signals over the vacant area. Routing over a vacant area will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

### 9.7.2.6 Board Design

The following recommendations are based on a ground referenced design.

- **Top Layer Routing**  
Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity, and removes any impedance inconsistencies due to layer changes.
- **Ground Plane**  
A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.
- **Power Plane**  
Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply plane's VDD\_A. Analog power may be a metal fill "island," separated and RC filtered from digital power.
- **Signal Layer Routing**  
The digital high-speed signals, which include all of the LAN interconnect interface signals, must be routed on an internal signal layer away from the analog signals.

### 9.7.2.7 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs:

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are long. The magnetics should be as close to the connector as possible ( $\leq$  one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC), and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inch from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45/11, and the PLC.

- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have  $\sim 100\ \Omega$  impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between  $75\ \Omega$  and  $85\ \Omega$ , even when the designers think they've designed for  $100\ \Omega$ . (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by  $5\ \Omega$ – $20\ \Omega$ . A  $10\ \Omega$ – $15\ \Omega$  drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a capacitor is put in either of these locations. If a capacitor is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These capacitors are not necessary, unless there is some overshoot in 100 Mbps mode.

**Note:** It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

**Note:** Close should be considered to be less than 0.030 inch between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

### 9.7.3 Intel® 82562ET/EM Guidelines

For documentation on LAN, refer to [Section 1.1](#). For correct LAN performance, designers must follow the general guidelines outlined in [Section 9.7.2](#). Additional guidelines for implementing an 82562ET or 82562EM Platform LAN connect component are provided in the following sections.

#### 9.7.3.1 Guidelines for Intel® 82562ET/EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which can cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

#### 9.7.3.2 Crystals and Oscillators

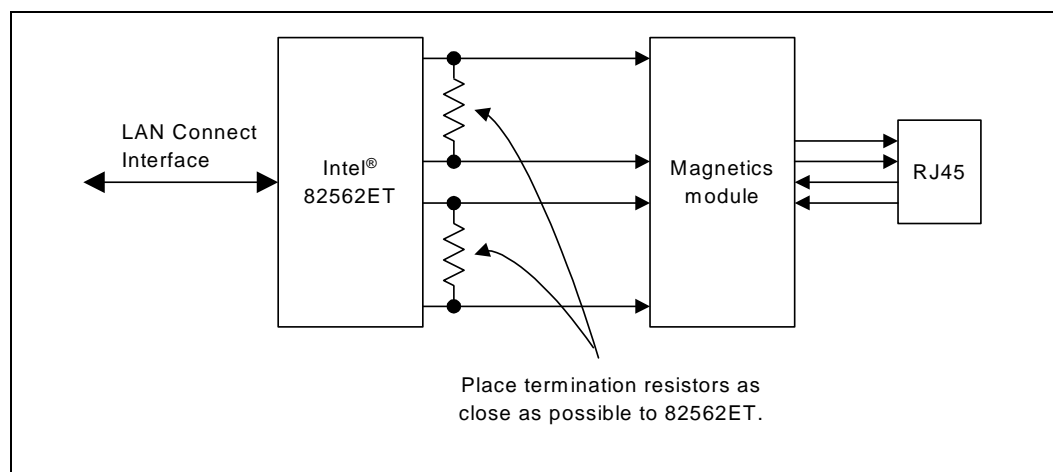
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility of radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible. Do not route any noisy signals in this area.

### 9.7.3.3 Intel® 82562ET/EM Termination Resistors

The  $100\ \Omega \pm 1\%$  resistor used to terminate the differential transmit pairs (TDP/TDN), and the  $121\ \Omega \pm 1\%$  resistor used to terminate the differential receive pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (82562ET or 82562EM) as possible. This is due to the fact that these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

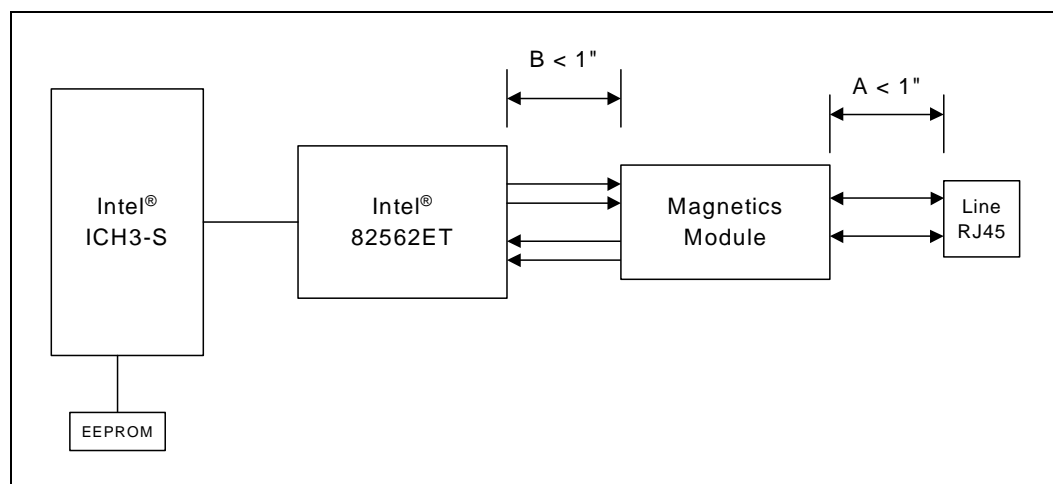
**Figure 9-19. Intel® 82562ET/EM Termination**



### 9.7.4 Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ45 connector to the magnetics module, and distance 'B' from the 82562ET or 82562EM to the magnetics module. The combined total distances A and B must not exceed 2 inches. (See [Figure 9-20](#).)

**Figure 9-20. Critical Dimensions for Component Placement**



### Distance from Magnetics Module to RJ45 (Distance A)

The distance A in [Figure 9-20](#) should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- **Differential Impedance:** The differential impedance should be 100  $\Omega$ . The single ended trace impedance will be approximately 50  $\Omega$ ; however, the differential impedance can also be affected by the spacing between the traces.
- **Trace Symmetry:** Differential pairs (such as TDP and TDN) should be routed with consistent separation, and with exactly the same lengths and physical dimensions (for example, width).

**Warning:** Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ45 as short as possible should be a priority.

**Note:** Measured trace impedance for layout designs targeting 100  $\Omega$  often results in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105  $\Omega$  – 110  $\Omega$  should compensate for second order effects.

### Distance from 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100  $\Omega$  differential value. These traces should also be symmetric and equal length within each differential pair.



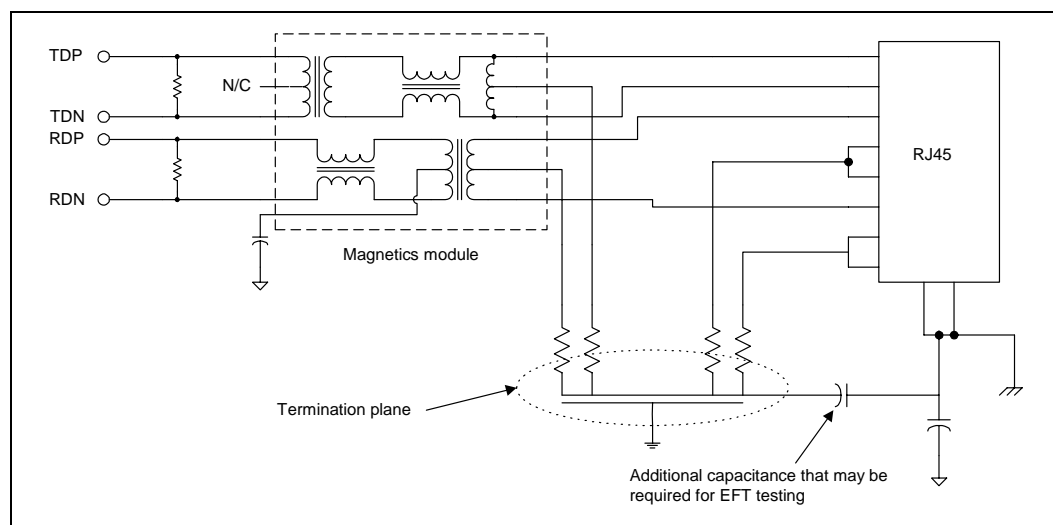
## 9.7.5 Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane, and couples capacitively to the ground plane creating the required 1500 pF of capacitance. The signals can be routed through 75  $\Omega$  resistors to the plane. Stray energy on unused pins is then carried to the plane.

### Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used to meet the EFT requirements, it should be rated for at least 1000 Vac.

Figure 9-21. Termination Plane



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# Debug Port

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# 10

The debug port design information can be found in a separate document. The routing of the signals, the signal levels, and all other information required to develop a debug port on this platform can be found in the *ITP700 Debug Port Design Guide*.

## 10.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the system bus of Intel Xeon processors. Contact Tektronix, Inc. and Agilent Technologies to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of these systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a system that can make use of an LAI: mechanical and electrical.

## 10.2 Mechanical Considerations

The LAI is installed between the processor socket and the microprocessor. The LAI pins plug into the socket, and the microprocessor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the microprocessor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system.

## 10.3 Electrical Considerations

The LAI also affects the electrical performance of the system bus. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that the tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution it provides.

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# EMI and Mechanical Design Considerations

# 11

## 11.1 Introduction

As microprocessor amperage and speeds increase, the ability to contain the corresponding electromagnetic radiation becomes more difficult. Frequencies generated by these processors will be in the low gigahertz (GHz) range, which will impact both the system design and the electromagnetic interference (EMI) test methodology.

This section is intended to provide electrical and mechanical design engineers with information that will aid in developing a platform that will meet government EMI regulations. Heatsink grounding, processor shielding, differential and spread spectrum clocking, and the test methodology impact to FCC Class B requirements are specifically discussed.

Designers should be aware that implementing all the recommendations in this guideline will not guarantee compliance to EMI regulations. Rather, these guidelines may help to reduce the emissions from processors and motherboards and make chassis design easier.

### 11.1.1 Brief EMI Theory

Electromagnetic energy transfer can be viewed in four ways: radiated emissions, radiated susceptibility, conducted emissions, and conducted susceptibility. For system designers, reduction of radiated and conducted emissions is the way to achieve EMC compliance. Susceptibility is typically not a major concern in the server environment, although it may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields), and magnetic (H-fields) waves traveling together and oriented perpendicular to one another. Although E- and H-fields are intimately tied together, they are generated by different sources. E-fields are created by voltage potentials, while H-fields are created by current flow. In a steady state environment (where voltage or current is unchanging), E- and H-fields are also static and of no concern to EMI. Changing voltages and currents are of concern since they contribute to EMI. If a dynamic E-field is present, then there must be a corresponding dynamic H-field, and vice versa. Motherboards with fast processors generate high frequency E- and H-fields from currents and voltages present in the component silicon and signal traces.

Two methods exist for minimizing E- and H-field system emissions: prevention, and containment. Prevention is achieved by implementing design techniques that minimize the ability of the motherboard to generate EMI fields. Containment is used in a chassis environment to contain radiated energy within the chassis. Careful consideration of board layout, trace routing, and grounding may significantly reduce a motherboard's radiated emissions and make the chassis design easier.

## 11.1.2 EMI Regulations and Certifications

Original Equipment Manufacturers (OEMs) ensure EMC compliance by meeting EMI regulatory requirements. System designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B.
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 Class B limits.

The FCC rules require any OEM that sells an “off-the-shelf” motherboard in the United States to pass an open chassis test. Open chassis testing is defined as removing the chassis cover (or top and 2 sides), and testing for EMI compliance (although permitted emission levels are allowed to be higher). Removing the cover greatly reduces the shielding provided by the chassis and increases the amount of EMI radiation. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI.

## 11.2 EMI Design Considerations

The following sections describe design techniques that may be applied to minimize EMI emissions. Some techniques have been incorporated into Intel-enabled designs (differential clock drivers, selective clock gating, etc.), and some must be implemented by motherboard designers (trace routing, clocking schemes, etc.).

### 11.2.1 Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking is defined as continuously ramping (or modulating) the processor clock frequency over a predefined range (see [Figure 11-1](#)). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see [Figure 11-2](#)). Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency along a predetermined path (or modulating profile). [Figure 11-1](#) shows an example of a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 kHz (above the audio band), and small enough not to upset system timings (less than 0.8% of the clock frequency). SSC has been demonstrated to effectively reduce peak radiation levels, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between  $f_{nom}$  and  $(1-\delta)*f_{nom}$ , where  $f_{nom}$  is the nominal frequency for a constant frequency clock. The “ $\delta$ ” specifies the total amount of spreading as a relative percentage of  $f_{nom}$ . The modulation percentage is always a function of  $1-\delta$  and not  $1+\delta$ , as increasing the clock frequency above the rated speed of the processor may cause unpredictable operation.

Figure 11-1. Spread Spectrum Modulation Profile

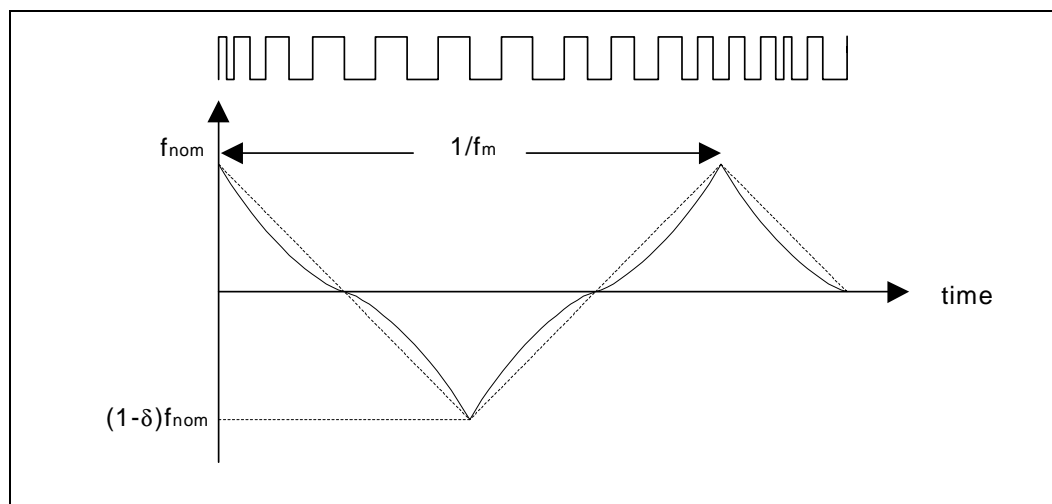
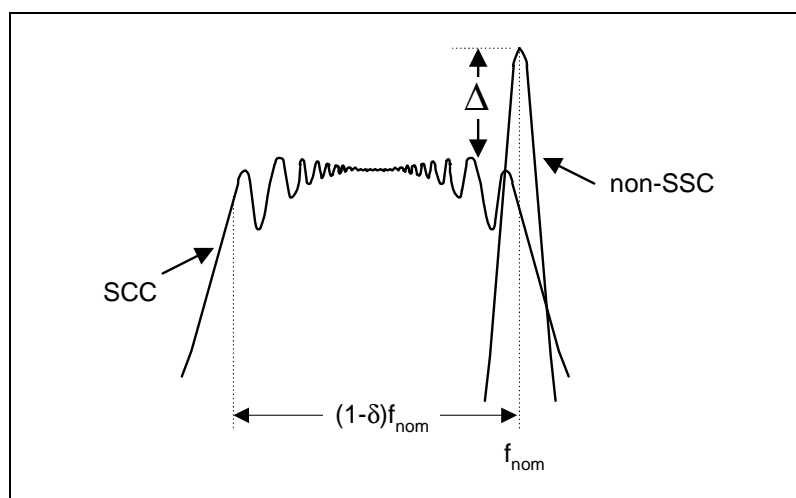


Figure 11-2. Impact of Spread Spectrum Clocking on Radiated Emissions

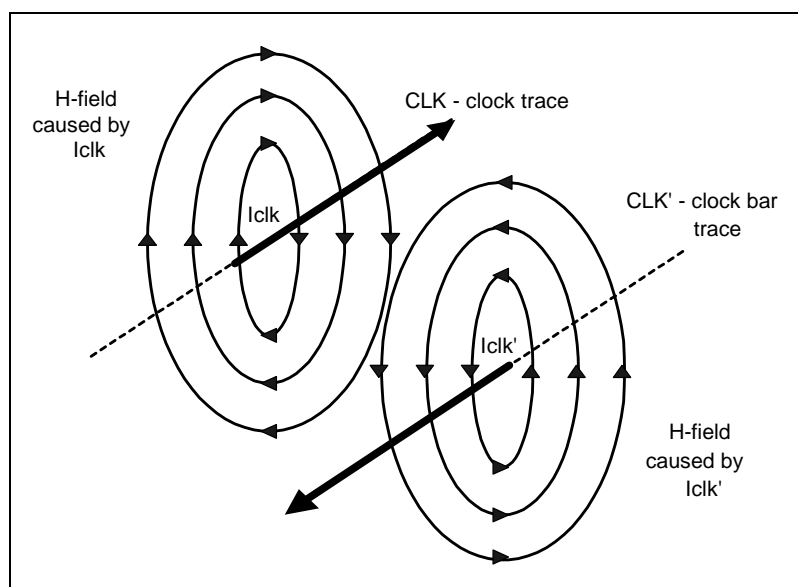


## 11.2.2 Differential Clocking

Differential clocking requires that the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock, and is also 180 degrees out of phase. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock and clock-bar signals.

EMI reduction due to differential clocking is caused by H-field cancellation. Since H-field orientation is generated by and is dependent upon current flow, two equal currents flowing in opposite directions and 180 degrees out of phase will have their H-fields cancelled (see [Figure 11-3](#)). Lower H-fields will result in reduced EMI radiation.

Figure 11-3. Cancellation of H-fields Through Inverse Currents



Differential clocking can also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.), and radiate noise that has been induced onto them. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise will appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched, and spacing between the two traces should be kept as small as possible. This will minimize loop area and maximize H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair should be the same. Also, the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias should be less than  $\frac{1}{4}$  of a wavelength of the fifth harmonic of the processor core frequency.

### 11.2.3 PCI Bus Clock Control

Experimental data has indicated a reduction in EMI may be possible by disabling the clocks to unused (and therefore unterminated) PCI slots. CK408B, the clock chip that has been specified and designed for this platform, supports individual control of the various PCI clocks. Designers have the option to enable or disable individual PCI clocks depending upon their specific system configuration requirements. Refer to the *CK408B Clock Synthesizer Design Guidelines* for details on how to configure the PCI clocks.



### 11.2.4 Heatsink Effects

Heatsink grounding may be an effective way to reduce system EMI emissions. Noise coupled from the processor package to the heatsink may cause it to act as an antenna and re-radiate the noise. Heatsink size, shape, fin pattern, orientation and material may all impact its ability to reradiate the high frequency signals. Designers will have to experimentally investigate the behavior of a particular heatsink to determine its EMC performance.

Grounding of the heatsink through the processor package is not possible with the current package implementation, but may be an option at some time in the future. Therefore, system designers must either design their own heatsink grounding solution, or use the heatsink grounding device described in [Section 11.2.5](#).

When designing a grounding mechanism for the heatsink, care must be taken to minimize the impedance and distance between the ground paths. Typical guidelines suggest ground points should be separated by less than  $\frac{1}{4}$  wavelength of the third harmonic of the processor core frequency.

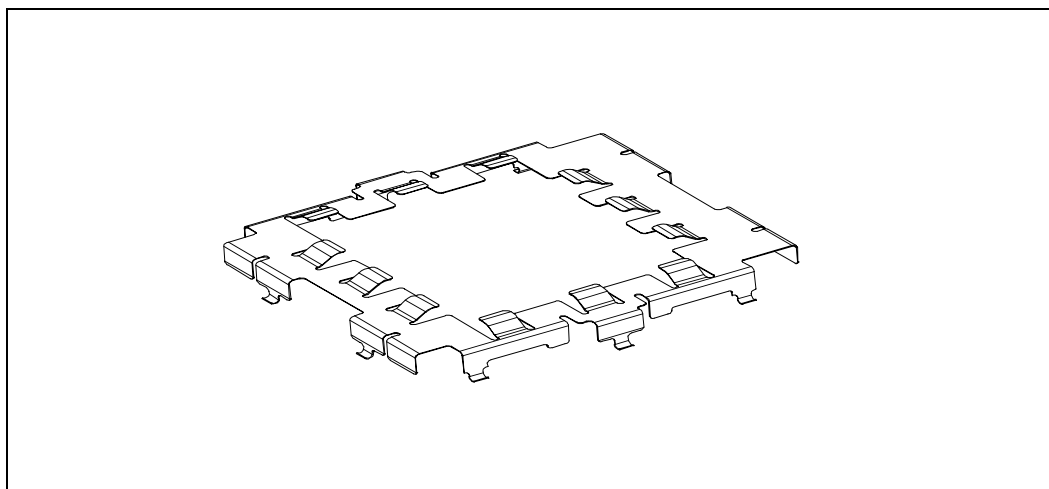
Grounding materials should be selected to eliminate galvanic action between the various metals in contact. Oxidation of the various materials should also be considered because some oxides are non-conductive (for example, aluminum oxide), and will degrade EMC performance over time. Manufacturing process residue or coatings to prevent oxidation should also be checked for conductivity, especially at high frequencies.

### 11.2.5 EMI Ground Frames and Faraday Cages

Grounding of heatsinks may reduce EMI, but that alone may not be sufficient to pass the required tests. Additional shielding of the processor itself may be necessary. A Faraday cage placed around the processor may provide a reduction in radiated noise and make chassis design easier.

A true Faraday cage would completely surround the source of radiation and contain all radiated energy. Within the limitations of processor packaging and motherboard assembly, it is not possible to create a true Faraday cage around the processor. By using the heatsink and motherboard ground plane as two sides of the cage and a metal frame to enclose the remaining four sides, a reasonable approximation of a Faraday cage can be achieved.

Intel has designed a “picture frame” type of grounding device, called an EMI ground frame, that fits between the processor and heatsink (see [Figure 11-4](#)). With this implementation, it is unnecessary to design a separate heatsink grounding mechanism because the frame will provide this capability. OEMs who choose to use the Intel designed grounding frame will need to provide ground pads on the top layer of the motherboard around the processor socket. These pads will provide the necessary ground continuity to complete the Faraday cage. Exact physical dimensions of the frame and the material used are provided in the processor IGES and Pro-E models for enabled components. The required motherboard ground pad descriptions are provided in [Section 11.3](#).

**Figure 11-4. Conceptual Processor Ground Frame**

### 11.2.6 EMI Test Capabilities

FCC regulations in the United States specify the maximum test frequency for products with clocks in excess of 1 GHz is five times the highest clock frequency or 40 GHz, whichever is lower. OEMs are advised to inquire into the capabilities of their preferred EMC test lab to ensure they are able to scan up to the required frequency range.

Processor performance and frequency double approximately every two years. With this in mind, it is advisable to be prepared for the frequencies that will need to be scanned in the next few years.

Since the FCC rules ultimately require testing to 40 GHz, commercial test equipment has been developed that is capable of making measurements to that frequency. Although it will be some time before processors require testing at this frequency, it may be cheaper to upgrade to 40 GHz now, rather than making several intermediate steps.

It is also possible to upgrade various parts at different times. The spectrum analyzer may be upgraded to 40 GHz today with only the necessary antennas to support the initial processor frequencies. As processor speed increases, the necessary antennas and cables can be purchased that support testing to the higher levels.

## 11.3 Retention Mechanism Placement and Keep-Outs

The retention mechanism (RM) for the Intel Xeon processor requires two keep-out zones: one for the EMI ground pads, and another for a limited component height area under the RM as shown in Figure 11-5. Figure 11-6 shows the relationship between the RM mounting holes and pin one of the sockets; it also documents the ground pads and keep-outs. Figure 11-7 details the ground pad locations and the associated limited height areas due to the ground frame.

The EMI ground pads under the retention mechanism must each have a minimum of eight vias connecting the pad to the baseboard ground plane. The retention holes must be non-plated. It is not necessary to have a ground pad on the secondary side of the baseboard when using the push-pin fasteners. The push-pins protrude approximately 0.200 inch from the secondary side of the board.

The ground pads for the EMI ground frame must have a minimum of six vias each connecting the pads to the ground plane. The suggested via size is 12 mils. This allows sufficient clearance to route traces between the vias on the secondary side of the PCB or on internal layers.

**Figure 11-5. Retention Mechanism Outline and Ground Pad Detail**

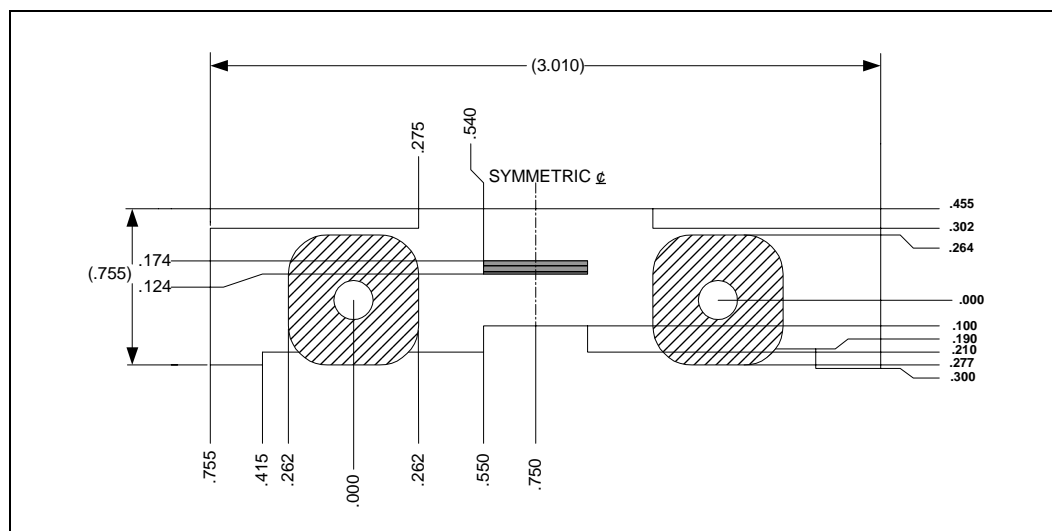
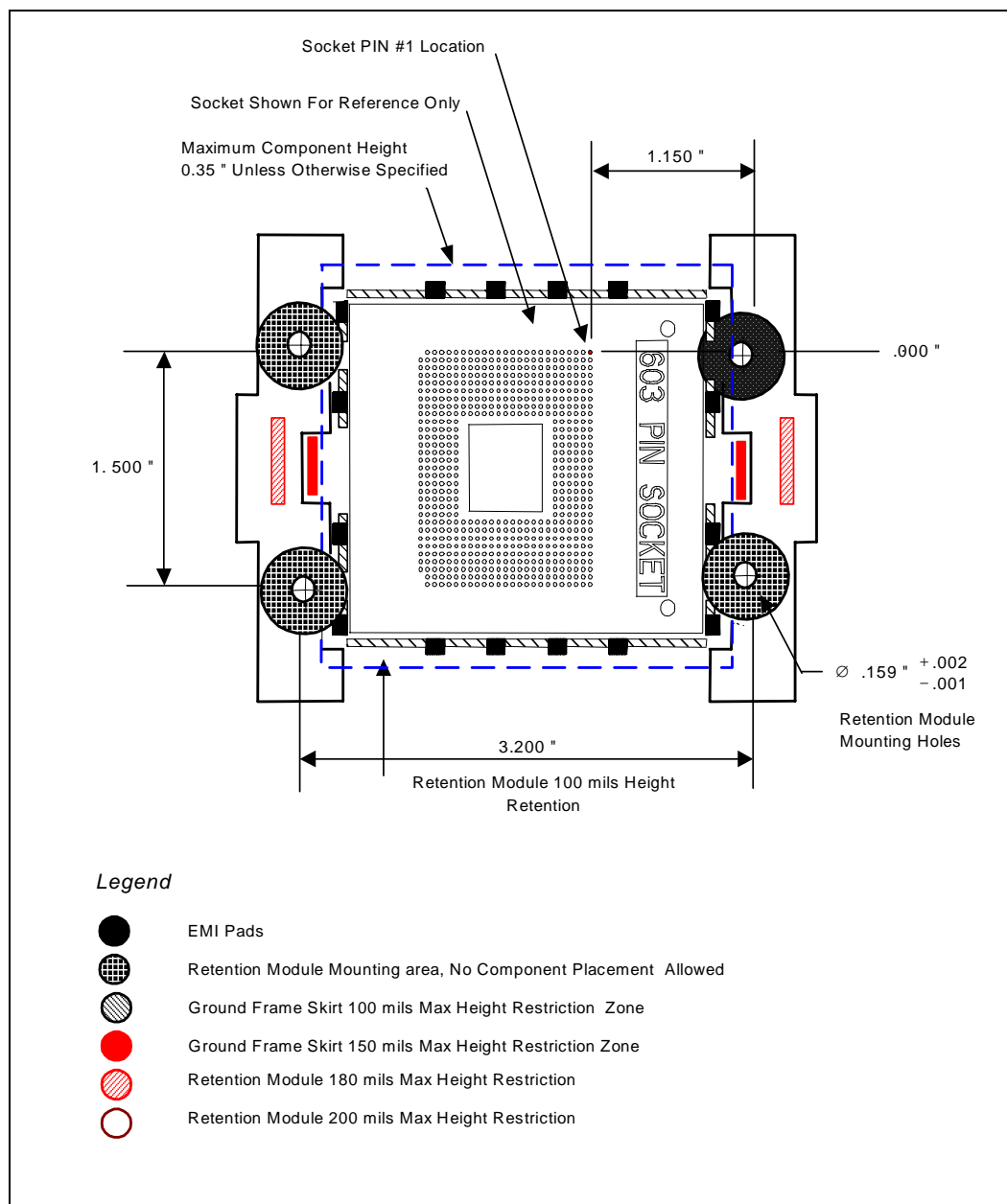


Figure 11-6. Retention Mechanism Placement and Keep-Out Overview

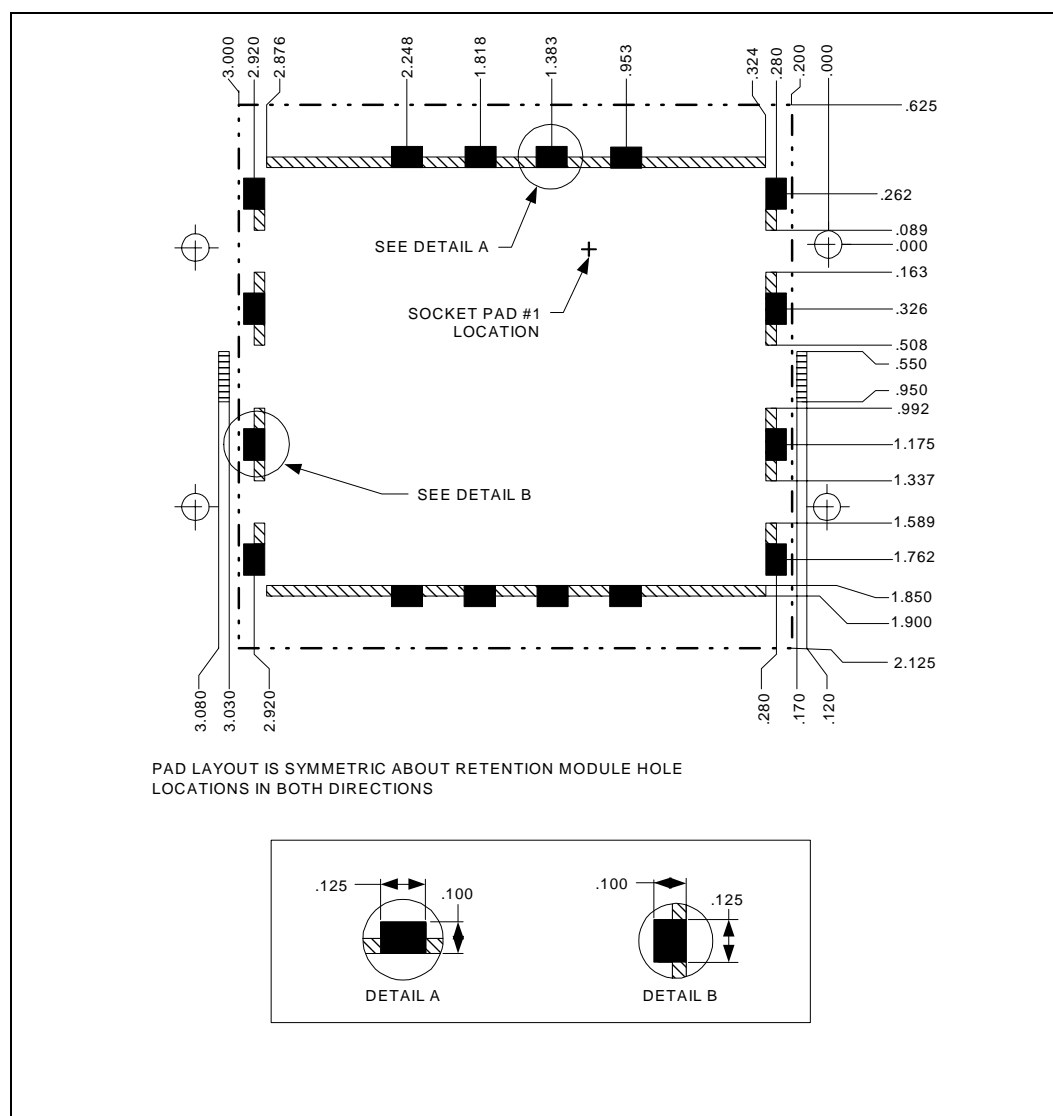


## 11.3.1 Grounding Techniques

In an effort to be proactive regarding electromagnetic interference (EMI) reduction, Intel is enabling a reduction technique for Intel Xeon processor-based systems. The solution is comprised of a metal grounding frame that contacts the heatsink on all four sides and provides grounding to the motherboard. A second, optional solution is the DC grounding strips, which provide the heatsink a two point electrical connection to ground and insert into the retention mechanism pieces.

The grounding frame for the Intel Xeon processor is meant to provide grounding of AC currents seen on the heatsink, and has been shown to be the most effective design in EMI reduction for the processor. The metal frame will be installed after the processor and retention mechanisms have been inserted. It will fit around the processor and inside of the retention mechanisms. Fingers on the top of the metal frame will provide contact to the heatsink, and fingers along the bottom will contact the ground pads on the motherboard. The grounding frame will require the placement of a series of ground pads surrounding the processor, as shown in Figure 11-8.

Figure 11-7. EMI Ground Size and Location

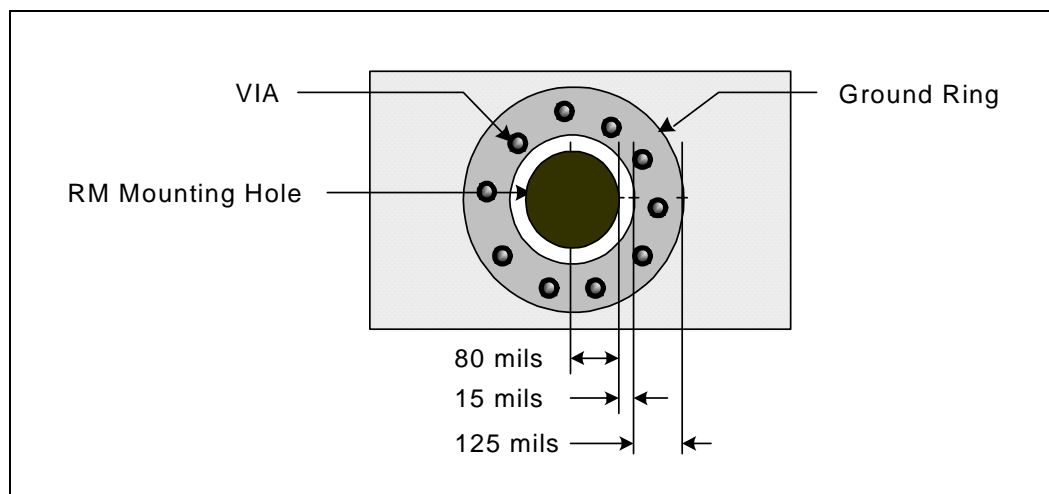


Utilization of the DC grounding strips requires ground pads around the mounting holes for the retention mechanism. Metal inserts will be pre-assembled to the retention modules to establish DC contact between heatsink base plate and the motherboard ground. The inserts will be grounded to the baseboard at mounting hole ground pads. Fingers on top of the insert will connect to the base of the heatsink. The requirements for the DC grounding insert are as follows:

- All four RM mounting holes must have ground pad rings.
- Ground pad annular ring should be no less than 125 mils wide. Try to cover the entire keep-out zone, if possible. See [Figure 11-8](#) for better dimensions.
- Place 8–12 vias in the annular ring, which connects the pad to internal ground planes.
- Anodizing or any form of insulated coating of the heat sink is strongly discouraged.

Refer to [Figure 11-8](#) for specific details regarding the required ground pads.

**Figure 11-8. Retention Mechanism Ground Ring**



# Platform Power Delivery Guidelines 12

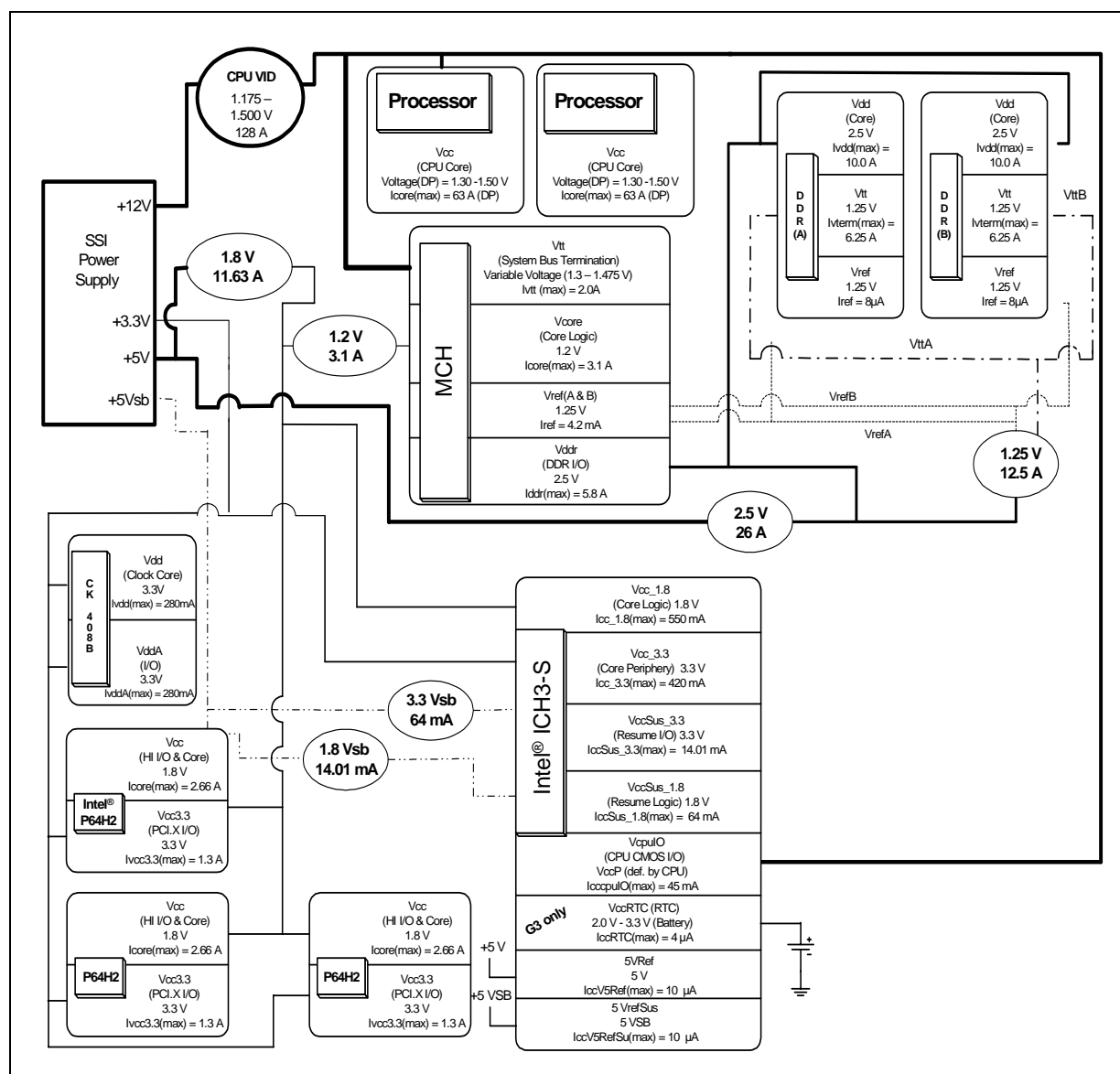
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This chapter depicts an example for board power delivery and the power requirements for some board components.

## 12.1 Customer Reference Board Power Delivery

Figure 12-1 shows the power delivery architecture for the E7500 Chipset Customer Reference Board.

Figure 12-1. Power Delivery Example



**NOTE:** The examples given in this Design Guide are only examples. Many power distribution methods achieve similar results. It is critical, when deviating from these examples in any way, to consider the effects of the change.



## 12.1.1 Processor Core Voltage

The processor core voltage power plane is used to power the processors. The processor core voltage operates between 1.30 V and 1.50 V. A VRM 9.1 compatible design is required for all Xeon platforms. The Voltage Regulator solution can be either a VRM 9.1 or a VRDown design. Refer to the *Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines*, *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines*, and *603 Pin Socket Design Guidelines* for more information.

## 12.1.2 2.5 V

The 2.5 V power plane is used to provide power to the DDR DRAM core, the MCH DDR IO ring, and reference voltage to the 1.25 V switching regulator. The 2.5 V power plane is created using a switching regulator, which should be able to support up to 26 A of current. This switching regulator receives its input directly from the 5 V power rail of the power supply. The DDR DRAM core requires at most 20.0 A of current. This value is a worst-case current, and is based on DRAM vendor specific specification for maximum current. Power levels will vary. In some cases, current requirements may be less than half of this maximum value, but a maximum current level of 20 A should be used to allow interoperability among DRAM devices. The current dedicated for VDD in the MCH is 5.8 A. This regulator is required in all designs.

## 12.1.3 1.25 V

A voltage regulator derived off 2.5 V produces two 1.25 V rails. One is for the MCH reference voltage (VREF); the other is for DDR termination voltage (VTERM). The switching regulator divides the 2.5 V power rail by 2 to drive 1.25 V reference voltage. This provides some common mode noise rejection between the DDR termination and I/O voltages. The entire power plane requires about 12 A of maximum current, and can be achieved by using either one or two regulators (one for both channels or one for each channel).

## 12.1.4 1.8 V

The 1.8 V power plane is created using a switching regulator sourcing from the 5 V power rail on the power supply. The 1.8 V plane powers the ICH3-S core logic, the 1.2 V regulator, and the hub interface I/O rings of the P64H2s. This voltage rail requires approximately 11.63 A maximum current. The hub interface on each P64H2 device consumes about 2.66 A. The hub interface on the ICH3-S device consumes about 550 mA of current. This regulator is required in all designs.

## 12.1.5 1.2 V

The 1.2 V power plane powers the MCH core logic. The MCH core logic requires 3.1 A. A switching regulator using either the 3.3 V or the 5 V power rail is the regulator's input to power the 1.2V plane.

## 12.1.6 5 VSB

The 5 VSB power plane comes directly off the 5 VSB power rail and has two functions, to provide power to resume functions via a 3.3 VSB regulator in I/O devices off of the ICH3-S, and to provide 1.8 VSB power through a linear regulator. The resume I/O segment of the ICH3-S requires 64 mA of current, while the 5 VSB-to-1.8 VSB regulator requires 14.01 mA.

## 12.1.7 3.3 VSB

The 3.3 VSB power plane is the output of a 5 VSB-to-3.3 VSB voltage regulator. The power plane is used solely for the resume I/O features of the ICH3-S. This segment is given only about 64 mA. This regulator is required in all designs.

## 12.1.8 1.8 VSB

As stated before, the 1.8 VSB provides power to the resume logic within the ICH3-S. This logic uses about 14.01 mA. This regulator is required in all designs.

## 12.1.9 Power Summary

The following table summarizes the platform power.

**Table 12-1. Power Summary**

Power Rail	Source	Destination	Max Current
CPU	VRM 9.1 / VRD	2 CPUs, MCH, Intel® ICH3-S	126 A
2.5 V	5 V switching regulator	MCH DDR	26 A
1.25 V	5 V to 2.5 V switching regulator	MCH DDR	12.5 A
1.8 V	5 V switching regulator	P64H2, ICH3-S	13.86 A
1.2 V	1.8 V switching regulator	MCH	3.1 A
5 VSB	Power Supply	3.3 VSB, 1.8 VSB	78 mA
3.3 VSB	5 VSB voltage regulator	ICH3-S	64 mA
1.8 VSB	5 VSB voltage regulator	ICH3-S	14.01 mA

## 12.2 Processor Power Distribution Guidelines

### 12.2.1 Processor Power Requirements

This section describes the requirements for supplying power to a Intel Xeon processor. For detailed electrical specifications, refer to the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet*. The processor will typically operate between VCC\_MID and VCC\_MAX. The processor allows the use of Auto HALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to specific internal sections of the processor and the BCLK depending on each particular state. This can create load-change transients as high as 450 amps per microsecond on VCC\_CPU at the socket pins. Note that the processor can also cause load changes of this magnitude while executing regular code. In this document, a load-change transient is a change from one current requirement (averaged over many clocks) to another. In the future, the processor may require higher currents and different voltages.

#### 12.2.1.1 Multiple Voltages

“VCC\_CPU” in this section refers to the processor core VCC, cache supply voltage, and Assisted Gunning Transceiver Logic + (AGTL+) supply voltage. In the processor, the core and cache are on the same silicon and are powered from the same power plane—unlike Pentium II Xeon and Pentium III Xeon processors, which required different power planes.

For the processor,  $VCC_{MAX} = 1.500\text{ V}$  and  $SM\_VCC\_CPU = 3.3\text{ V}$ . The  $VCCA$  supplies power to the processor core and on-die termination used for the AGTL+ bus.

$VCCIOPLL$ ,  $VCCA$ , and  $VSSA$  are the power supplies to the internal PLL.  $VCCIOPLL$ ,  $VCCA$  and  $VSSA$  must be connected to  $VCC\_CPU$  through a discrete RLC filter as described in [Section 12.2.8](#). Refer to the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet* for the pin location of these voltages.

### 12.2.1.2 Voltage Tolerance

Refer to the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet* for voltage tolerance specifications. Failure to meet these specifications on the low-end tolerance results in transistors slowing down and not meeting timing specifications. Not meeting the specifications on the high-end tolerance can cause damage or reduce the life of the processor.

Unlike the previous Intel processors (the Pentium III Xeon processors), the Intel Xeon processor specifications for  $VCC\_CPU$  and  $ICC$  are not independent. The VID definition is changed to absolute maximum  $VCC\_CPU$  allowed.  $ICC\_MAX$  is measured at  $VCC\_MAX$ .

## 12.2.2 Processor Current Requirements

The processor allows the use of low power states to reduce power consumption by stopping the clock to specific internal sections of the processor and the BCLK depending on each particular state. This can create load change transients as high as 450 amps per microsecond (450 A/ $\mu$ s slew rate) on  $VCC\_CPU$  at the socket pins. The shape of the current through the processor socket during a transient usually does not have a constant slope due to the high-frequency filtering by the package decoupling. [Table 12-2](#) shows the maximum current and current step size per processor.

**Table 12-2. Processor Current Step Parameters**

Processor Frequency	Maximum Step Size per Processor	Maximum Current per Processor
1.8 GHz	26.5 A	41.9 A
2.0 GHz	29.3 A	44.7 A
2.2 GHz	32.1 A	47.6 A
FMB	46.3 A	61.5 A

## 12.2.3 Power Delivery Layout Requirements

Note that the Voltage Regulator must be placed as close as possible to the processor, on the side of the socket that has the greatest density of power and ground pins.

The maximum distance between each processor and its voltage regulator module or the output inductors of an embedded Voltage Regulator should not be greater than 1.5 inches. To be more specific, the distance between the facing edges of the Voltage Regulator connector and the socket should be no more than 0.5 inch.

Processor  $VCC\_CPU$  static and transient tolerances and the corresponding Voltage Regulator tolerances assume power distribution paths with resistances no greater than 0.4 m $\Omega$  and inductances no greater than 0.1 nH. Meeting these limits can be a challenge because of system layout constraints.

For an 8-layer board, refer to [Figure 3-2](#) in which the ground planes are used as signal reference planes. If cost is the main consideration, you may opt to design a platform using fewer layers. In that situation, a thorough analysis is recommended.

Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone.

Because processor voltage is unique to most system designs, a voltage island is probably be the most cost-effective means of distributing power to the processors. This island should not have any breaks from the source of power to the load to minimize inductance in the plane. It should completely surround all of the pins of the source and all of the pins of the load.

Intel recommends a 2 oz. copper power plane for VCC\_CPU, and a 2 oz. copper power plane for VSS. This can be implemented on two 1 oz. copper layers or four 1/2 oz. copper layers. The bulk capacitors can be placed close to the processors, and the high-frequency capacitors should be placed next to the processors. Distribute the bulk and high-frequency capacitors equally on both sides of the socket where the power/ground pins are located (the east and west side).

The Intel Xeon processor socket has 603 pins with 50 mil pitch. The routing of the signals, power, and ground pins require creation of lots of vias. These vias cause a “Swiss cheese” effect in the power and ground planes beneath the processor, resulting in increased inductance of these planes. It is recommended that you place as many high-frequency capacitors as possible inside the cutout of the processor socket. The remaining high-frequency capacitors should be placed next to the processor, specifically near the power/ground pins.

The data bus must route over a uniform power plane because of signal quality constraints. Consequently, in a multiprocessor system design, a single power plane should be used for power delivery to all processors. Multiple processors operating at different voltages are not supported, and will not be validated by Intel.

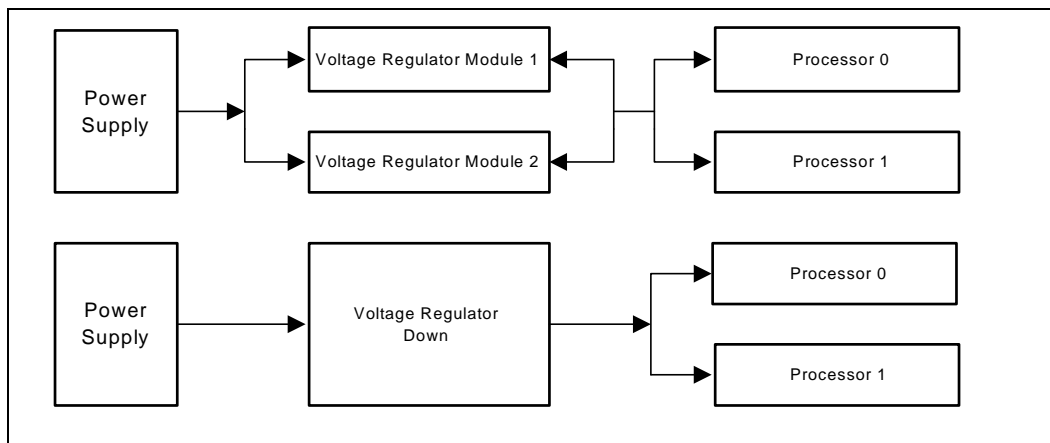
System boards can include a SENSE input for each Voltage Regulator. The trace resistance should not be greater than 1.0  $\Omega$ . The sense pins do not draw current, therefore no voltage drop exists. Route the SENSE trace as follows:

- In a DP system, the SENSE lines from the VR should be routed to a point between and equidistant from all processors. At this point, tie all SENSE lines together and connect to VCC\_CPU. This will allow for proper current sharing between the VRs.
- The processor VCCSENSE and VSSSENSE pins must be routed to vias. The vias should be as close to the socket pins as possible, and should be connected with low impedance traces. Because these signals provide measurement points to verify adherence to the processor's VCC\_CPU specifications, the vias need to be accessible to measurement equipment. These pins must not be used as SENSE lines to the VRs.

## 12.2.4 Voltage Regulator Requirements

Intel requires a local VRM 9.1-compliant Voltage Regulator for VCC\_CPU. As shown in [Figure 12-2](#), it can be either one Voltage Regulator Module (VRM 9.1) DC-to-DC converter for each processor, or one Voltage Regulator-Down (VRD) solution for both processors in a DP system. Refer to either *VRM 9.1 DC-DC Converter Design Guidelines* or *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* for Voltage Regulator tolerance specifications (regulation requirements at the voltage regulator remote sense point located at the geometric center of the processors). These two documents are referred to as the voltage regulator guidelines.

**Figure 12-2. Power Distribution Block Diagrams for Two-Way System Motherboard**



The voltage regulator should be capable of accepting a 5-bit VID code, which is used to indicate the maximum voltage allowed by the individual processor unit. The VID values are documented in the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet*.

#### 12.2.4.1 Input Voltages and Currents

To minimize power distribution losses, the recommended main power source for the VR is 12 V +5%, – 8%. This voltage is supplied by a conventional server power supply such as the SSI EPS-12V. The system designer should ensure that the input circuit of the VR incorporates the necessary local bulk bypassing on the 12 V rail.

#### 12.2.4.2 Power Good Output (PWRGD)

The VR should provide an open collector or equivalent Power Good signal consistent with TTL DC levels. This signal should transition to the open (>100 kΩ) state within 10 ms of the output voltage stabilizing within the specified processor operating voltage range. The signal should be in the low impedance (to ground) state whenever VCC\_CPU is outside of the required range, and should be in the open state whenever VCC\_CPU is within its specified range. At power up, the PWRGD signal must remain in the low-impedance state until the output voltage has stabilized within the required tolerance.

The minimum voltage at which PWRGD is asserted should be the minimum VCC\_CPU specified in the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet*, minus margin to prevent false de-assertion, but at least 95% of (VID minus 125 mV). The maximum voltage at which PWRGD is asserted should be the VID set-point voltage, plus margin to prevent false de-assertion, but must be no greater than (VID plus 250 mV).

This PWRGD should be capable of sinking up to 4 mA while maintaining a voltage of 0.4 V or lower. When the output is in the open state, it should be capable of withstanding up to 5.5 V. Latch-up or damage cannot occur if the pull-up voltage on the system board is present with no +12 V input present. VR Power Good should remain low if the VR is disabled by the Output Enable (OUTEN) pin.

### 12.2.4.3 Fault Protection

When looking for a VR solution, you can look for some fault protection features. The features help the VR to prevent damage to itself and the circuits it powers. The VR should provide over-voltage protection (OVP) by including a circuit, separate from the voltage sense path, capable of shutting off the output drive when the output voltage rises beyond  $V_{trip}$ . The power input (12 V) should be protected with a fuse rated not greater than 30 A that sustains all operating and inrush conditions, and that “blows” only for catastrophic failure of the VR. The VR should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. If the VR goes into a shutdown state due to a fault condition on its output (not an internal failure), it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

## 12.2.5 VR Module 9.1 Recommendations

Intel has defined VRM 9.1 for supplying VCC\_CPU power to Intel Xeon processor based systems. The VRM 9.1 definition includes Remote-Sense, Current Share, and Output Enable features. VRM 9.1 suppliers must provide these features and must meet voltage and current requirements set forth in the *VRM 9.1 DC-DC Converter Design Guidelines*.

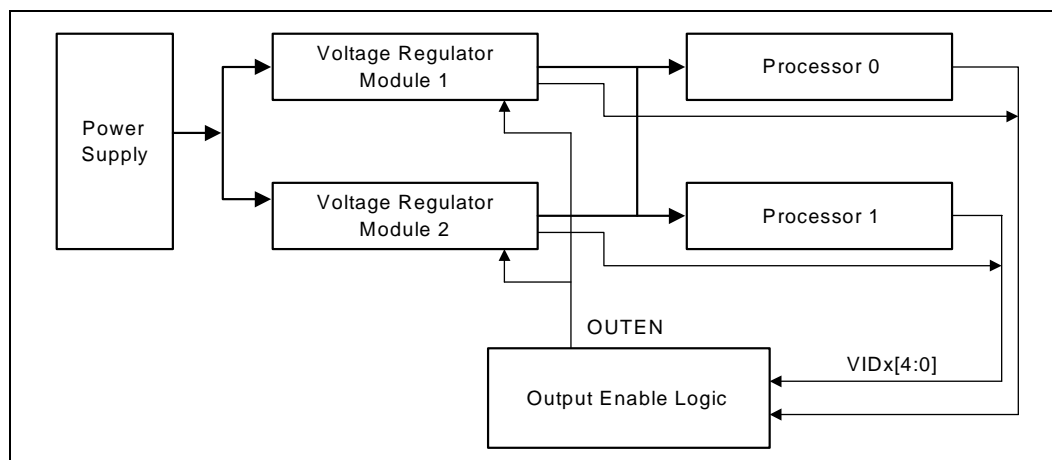
The VRM 9.1 Module, which provides VCC\_CPU supply to the Intel Xeon processor, has the capability of supplying a broad range of voltages (+1.1 V to +1.85 V).

It is highly desirable in DP applications that a current-sharing capability be available. The VRM 9.1 covers the specification for supporting this feature. A VRM 9.1 designed for current sharing must be capable of continuously producing a current that is higher than the rated value by a factor of half of the current sharing accuracy. For example, if a particular VRM 9.1 is designed to supply a 50 A processor as a maximum with 10% accuracy, the difference between the output currents of two or more VRM 9.1s in parallel may be as much as 5 A at any value of current actually produced, even to the point where one VRM 9.1 is producing 5 A, and one in parallel with it is producing no current in supplying a 5 A load. This is necessary to insure that the higher-current VRM 9.1 in a current-sharing pair does not operate above its limits due to current sharing errors. One pin of the VRM 9.1 is reserved for current sharing control for a VRM 9.1 designed for star-point or single-wire current sharing, i.e., Ishare. This pin will be connected to other VRM 9.1s within the system.

The VRM 9.1 output slew rate is specified at 50 A/ $\mu$ s. The slew rate for the Intel Xeon processor is 450A/ $\mu$ s at the socket pins. The system designer must provide adequate bulk and high-frequency decoupling on the motherboard to meet the appropriate processor required slew rate.

Figure 12-3 shows the recommended implementation of logic for monitoring the VID pins of all processors. This logic will determine that all of the installed processors are requesting the same VCC. If mixed voltage processors are detected, the output enable signal (OUTEN) of all VRM 9.1s must be disabled. Note that if a processor is not installed, the VID[4:0] of that processor are all high, and this should not cause disabling of the output of other VRM 9.1s. The VID lines must be pulled up internally in the VR.

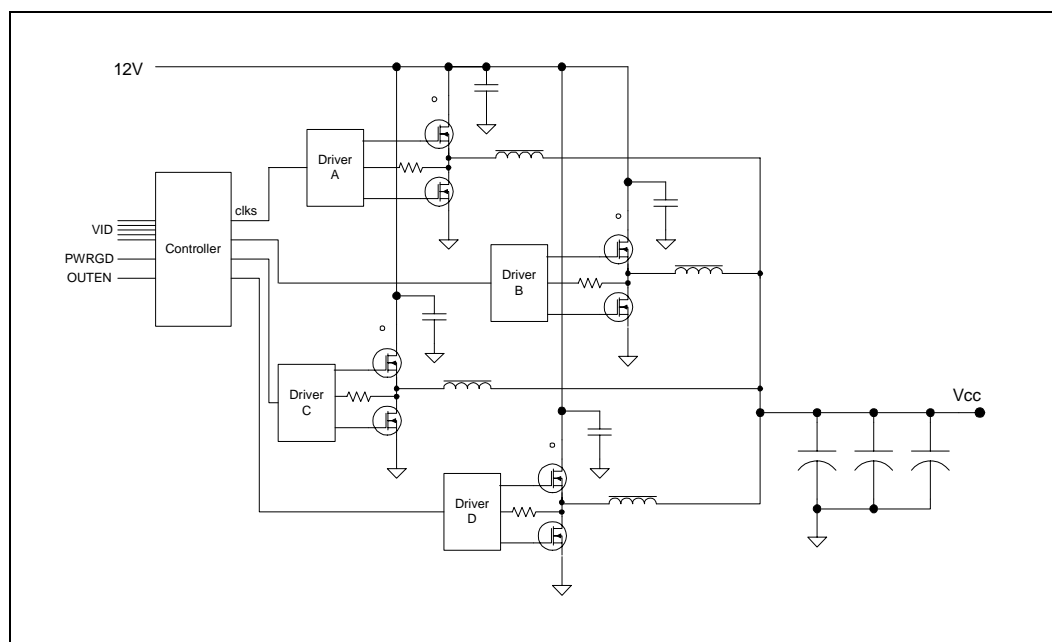
Figure 12-3. VRM VID Routing



## 12.2.6 VR Down Recommendations

Figure 12-4 is a simplified block diagram of a four-phase, interleaved VRD implementation.

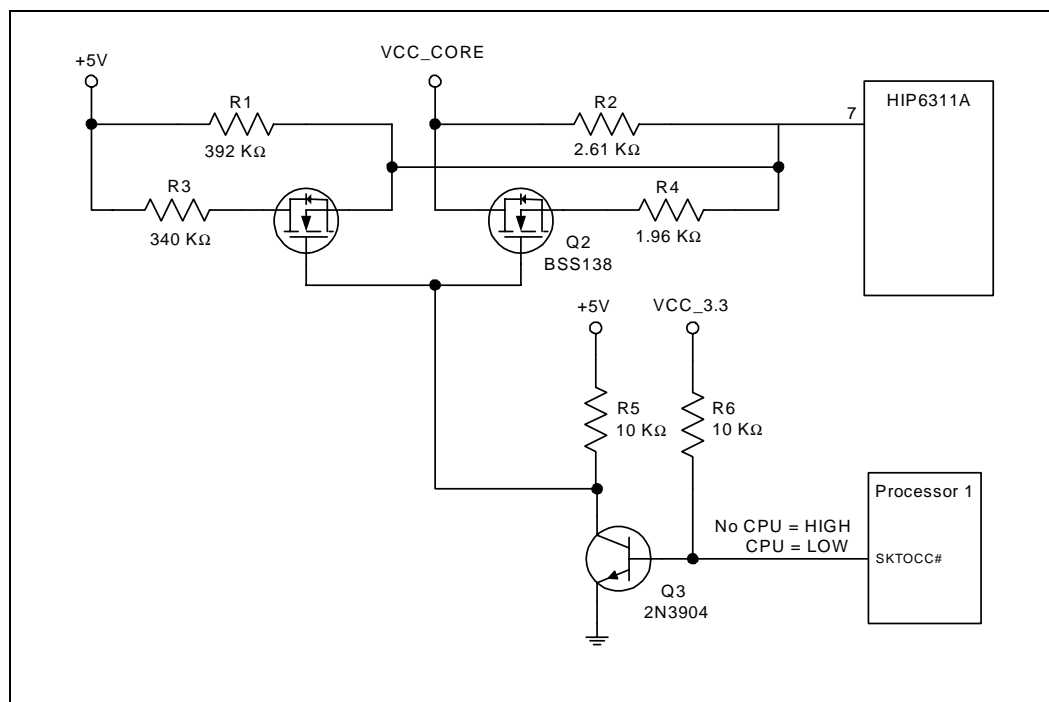
Figure 12-4. Simplified VRD Circuit Example



### Single or Dual Processor Operation

Many OEMs require that a dual-processor VRD supplying an Intel processor's common voltage plane operate with either one or two processors installed on the board (i.e., the design must meet the static and transient voltage characteristics of both the dual- and single-processor load lines). A solution is to adjust the load line for the number of installed processors. OEMs that want jumper-free systems can do this with logic that detects the presence of processors in each of the sockets, and selects resistor combinations to produce the right slopes. For example: no processors (00) = disable VRD; one processor (01 or 10) = single-processor load line; both processors (11) = dual processor load line.

**Figure 12-5. Example Load Line Selection Circuit**



The theory of operation of the dual processor load line selection circuit is straightforward. If a second processor (Processor 1) is not present, then the base of Q3 will be pulled high. This will cause Q3's collector to go to ground, turning off Q1 and Q2. The VCC\_CPU voltage will then go through R2 (droop resistor) to pin 7 (FB) of the HIP6311A controller. The offset voltage comes from the +5 V source through R1 into pin 7 of the controller. R3 and R4 will have no effect.

If a second processor is present, then the base of Q3 will be pulled low and Q3's collector will be high, turning on Q1 and Q2. The droop resistor, R2, will now be paralleled by R4, providing the droop required for a two-processor system. The offset resistor, R1, will be paralleled by R3 providing the offset for a two-processor system.



## 12.2.7 Voltage Sequencing

When designing a system with multiple voltages, there is always the issue of ensuring that no damage occurs to the system during voltage sequencing. Voltage sequencing is the timing relationship between two or more voltages such as VCC\_CPU and SM\_VCC.

SM\_VCC is required for correct operation of the Intel Xeon processor VID logic. The Intel Xeon processor's VID outputs use an active driver. A 3.3 V source connected to the processor's SM\_VCC pins supplies the VID output devices. As shown in Figure 12-7, the VID outputs will be valid within 10 ms after the 3.3 V supply reaches 95% of its nominal value. The system power supply should generate PWR\_OK no less than 100 ms after all of its outputs reach their respective 95% values. PWR\_OK may be used to enable the VR output. For example a supply adhering to ATX12V design guidelines meets this requirement. The VR's PWRGD output may be used to generate the PWRGOOD input to the processor. PWR\_OK should be de-asserted when any output of the supply falls below 95% of its nominal value (also consistent with ATX12V). It is important to maintain SM\_VCC anytime the output of the VR is enabled. Driving the VR's OUTEN control input with the PWR\_OK signal will ensure correct sequencing at both power-up and power-down.

Figure 12-6. VID Routing

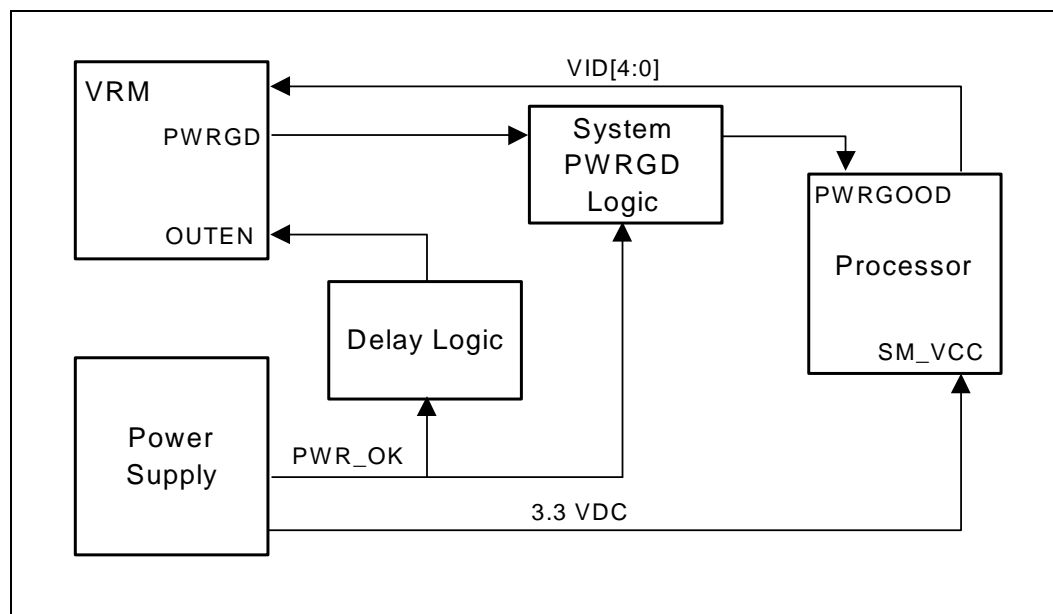
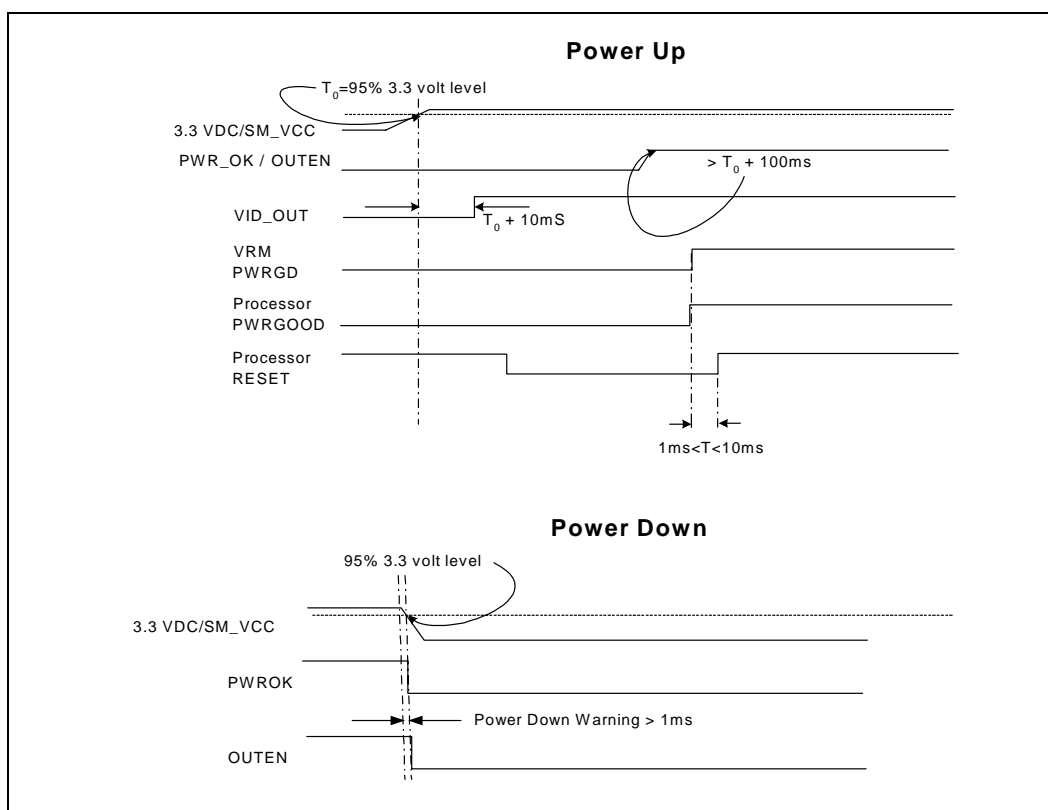


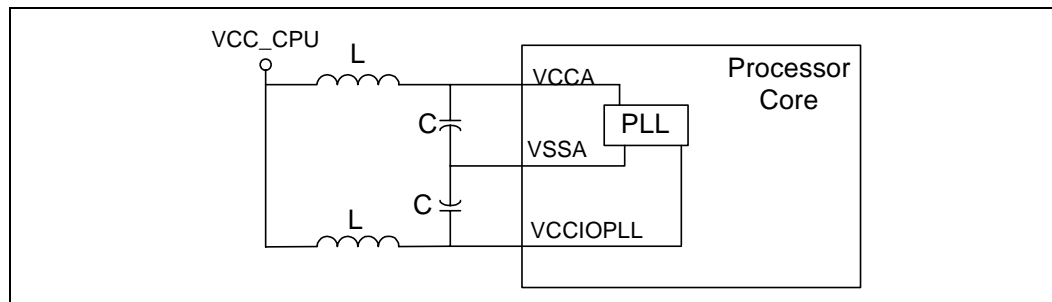
Figure 12-7. Power-Up and Power-Down Timing



## 12.2.8 VCCA, VCCIOPLL, and VSSA Filter Specifications

VCCA and VCCIOPLL are required by the processor's internal PLL. These voltages are created by using a low pass filter on VCC\_CPU. The processor has internal analog PLL clock generators that require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). The filter topology is shown in Figure 12-8. Not shown in the figure are the parasitics of connecting traces, circuits, and components.

Figure 12-8. Processor Filter Topology



The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation; it also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, we are addressing the recommendation for VCCA filter design. The same characteristics and design approach is applicable for VCCIOPLL filter design.

Other requirements:

- Use shielded type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.
- DC voltage drop from VCC\_CPU to the processor interposer pin VCCA should be < 33 mV, which in practice implies series  $R < 1.1 \Omega$ ; this also means pass band (from DC to 1 Hz) attenuation < 0.5 dB for VCC\_CPU = 1.1 V, and < 0.35 dB for VCC\_CPU = 1.7 V.

Table 12-3 and Table 12-4 list some recommended components for the filter. Values in the table are for reference only. For specific vendor information, contact your preferred vendor.

Table 12-3. Component Recommendation—Inductor

Part Number (Reference Designator)	Value	Tol	SRF	Rated I	DCR
TDK MLF2012A4R7KT	4.7 $\mu$ H	10%	35 MHz	30 mA	0.56 $\Omega$ (1 $\Omega$ max)
Murata LQG21N4R7K10	4.7 $\mu$ H	10%	47 MHz	30 mA	0.7 $\Omega$ ( $\pm$ 50%)

Table 12-4. Component Recommendation—Capacitor

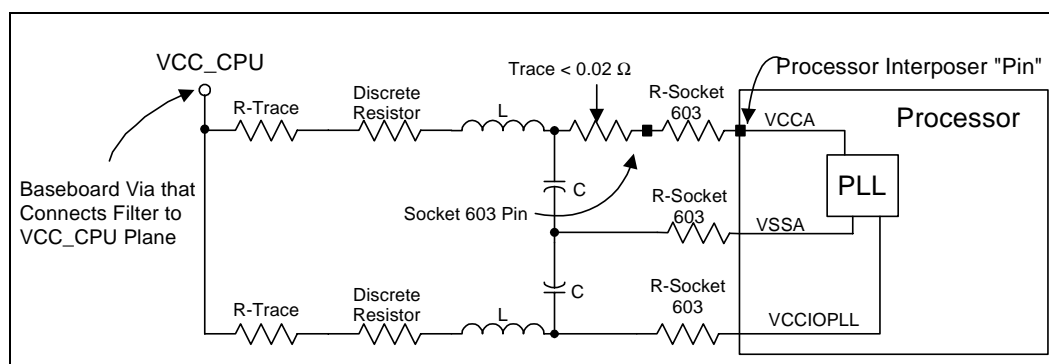
Part Number (Reference Designator)	Value	Tol	ESL	ESR
Kemet T495D336M016AS	33 $\mu$ F	20%	2.5 nH	0.225 $\Omega$
AVX TPSD336M020S0200	33 $\mu$ F	20%	TBD	0.2 $\Omega$

To satisfy damping requirements, total series resistance in the filter (from VCC\_CPU to the top plate of the capacitor) must be at least  $0.35\ \Omega$ . This includes the DCR of the inductor and any resistance (routing or discrete components) between VCC\_CPU and capacitor top plate. Keep the routing short and wide. If the total is less than  $0.35\ \Omega$ , add a discrete resistor to make up the difference. For example, if the selected filter inductor has a minimum of  $0.1\ \Omega$  DCR and a negligible routing resistance (less than  $10\ \text{m}\Omega$ ), add a discrete resistor of approximately  $0.3\ \Omega$ . The total maximum resistance in each route cannot be more than  $1.1\ \Omega$  as measured from VCC\_CPU (the baseboard via that connects the PLL filter to the VCC\_CPU plane) to the processor interposer pin. It is important to keep the total resistance of each of the PLL filter circuits on the motherboard no larger than necessary. [Figure 12-9](#) and [Figure 12-10](#) illustrate the recommended filter circuit. This path includes the total trace resistance (denoted “R-TRACE” in the following figures), discrete resistor (if needed), inductor DCR, and Socket 603 resistance ( $0.025\ \Omega$ ). It is important to note that “R-TRACE” includes the total trace resistance between VCC and the processor socket pin, but is represented in the figures as a single resistor to simplify the circuit representation.

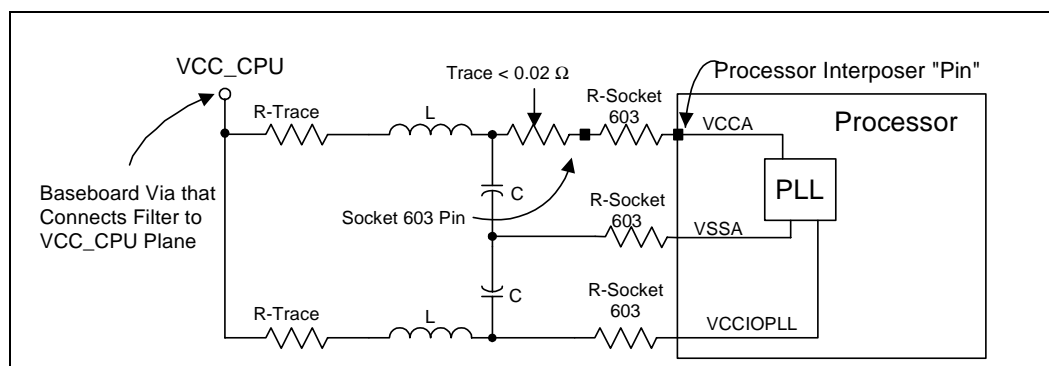
### Other Routing Requirements:

- C should be as close as possible to VCCA and VSSA pins in the socket (typically  $< 0.02 \Omega$  per route).
- Route away from clocks and fast switching signals.
- VCCA route should be parallel and next to VSSA route (to minimize loop area).
- VCCIOPLL route should be parallel and next to VSSA route (to minimize loop area).
- L should be close to C; any routing resistance should be inserted between VCC\_CPU and L.
- Any discrete R (if needed to meet minimum resistance) should be inserted between VCC\_CPU and L.

### Figure 12-9. Filter Implementation 1: Using Discrete Resistor



### Figure 12-10. Filter Implementation 2: No Discrete Resistor



### 12.2.9 Processor Decoupling

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance is bypassed. By bypassing the inductance of leads, power planes etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore, trade-offs must be made.

The Intel Xeon processor causes very large switching transients. These sharp surges of current occur at the transition between low power mode and high power mode. The designer must support a current slew rate of 450 A/μs at the socket pins. Larger bulk storage (CBULK), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react. A typical voltage converter has a reaction time on the order of 1 μs to 100 μs, while the processor's current steps are on the order of 100 ns to 200 ns. Bulk capacitance supplies energy from the time the high-frequency decoupling capacitors are drained, until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate that it is able to supply, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply.

A load-change transient occurs when coming out of or entering a low power mode. Load-change transients for the Intel Xeon processor are on the order of 55 A. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the STPCLK# pin is asserted or de-asserted, and during Auto HALT. Auto HALT is a low power state that the processor enters when the HALT op-code is executed.

**Note:** Note that even during normal operation (not STPCLK# or Halt), the processor current requirements can change by as much as 70% (± 10%) of the max current very quickly.

Maintaining voltage tolerance during these changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR), and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

#### 12.2.9.1 High-Frequency Decoupling

The system boards should include high-frequency capacitors as close to the socket power and ground pins as possible. Place as many capacitors as possible in the socket cut out area. [Table 12-5](#) lists the recommended high-frequency capacitance for Intel Xeon processor baseboards.

**Table 12-5. Processor High-Frequency Capacitance Recommendations**

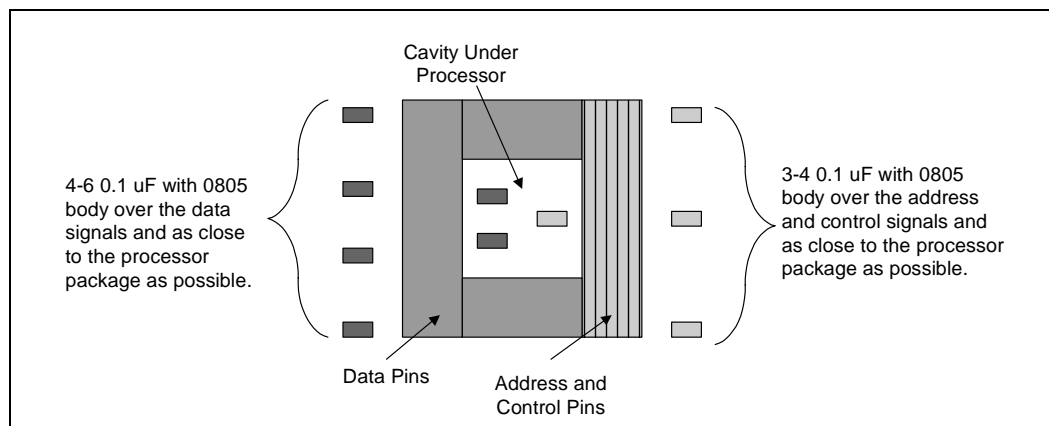
High-Frequency Capacitance	Quantity	ESR	ESL
0805 Package, 1 μF (Signal Integrity)	8	8 mΩ	702 pH
1210 Package, 22 μF (Power Decoupling)	20	10 mΩ	1.1 nH

If there is difficulty in placing the 1210 size 22 μF capacitors (as listed in [Table 12-5](#)), replace those with a same number of 1206 size 10 μF capacitors using similar placement guidelines. However, increase the number of OS-CONs (as defined in [Table 12-6](#)) from 9 to 10 to compensate for the reduced total capacitance.

In addition, high-frequency decoupling may be required for signal integrity. System boards designed using striplines with VCC\_CPU and VSS references should not require high-frequency decoupling beyond the recommendations listed in [Table 12-5](#). For systems using microstrip configurations, a return path discontinuity will exist between the processor and the baseboard due to the baseboard traces having only one reference plane. These systems should distribute decoupling capacitors, as shown in [Figure 12-11](#) and described as follows:

- 4 minimum, 6 preferred 1  $\mu\text{F}$  capacitors with 0805 packages distributed evenly over the data lines.
- 3 minimum, 4 preferred 0.1  $\mu\text{F}$  capacitors with 0805 packages distributed evenly over the address and control lines.

**Figure 12-11. Decoupling Example for a Microstrip Baseboard Design**

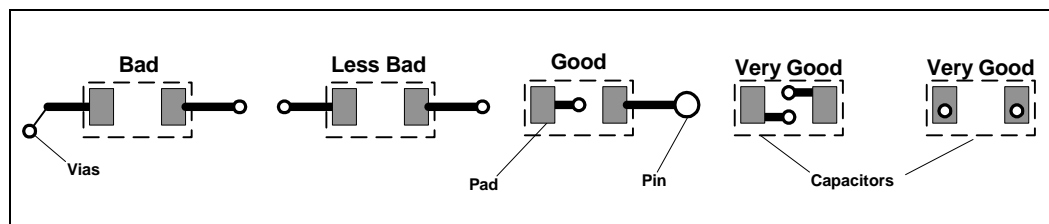


### Location of High-Frequency Decoupling

Place high-frequency decoupling as close to the power pins of the processor as physically possible. Use both sides of the board if necessary for placing components to achieve the optimum proximity to the power pins. This is vital because the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pins of the processor without the use of a via. [Figure 12-12](#) illustrates these concepts.

**Figure 12-12. 1206 Capacitor Pad and Via Layouts**



## 12.2.9.2 Bulk Decoupling

Table 12-6 lists the recommended bulk capacitance parameters for Intel Xeon processors. The following recommendations indicate the decoupling suggested for each processor in the system.

**Table 12-6. Processor Bulk Capacitance Recommendations**

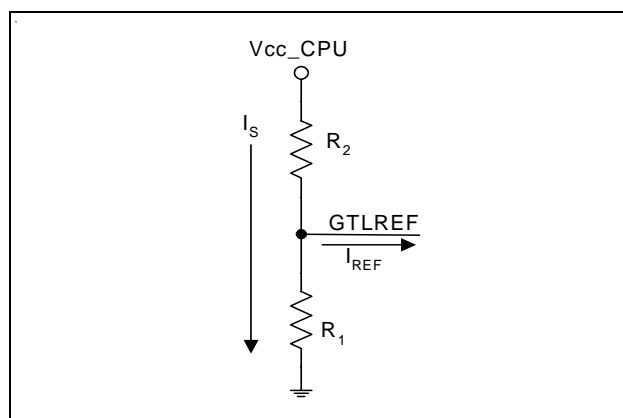
Design Type	Bulk Capacitance	Quantity	ESR	ESL	RMS Current Rating
On-board Design	OS-CON, 560 $\mu$ F	9	12 m $\Omega$	3.1 nH Max	5.04 Arms

Place some bulk decoupling on the baseboard as close to the processor socket as possible (maximum of 0.5 inch away). The location of bulk capacitance is not as critical as the high-frequency decoupling because more inductance is already expected for these components. However, good placement of these components will affect the transient response of the system for the better, as shown in simulation. Place the remaining bulk capacitors next to the voltage converter module.

## 12.2.10 GTLREF[3:0]

GTLREF[3:0] are low current inputs (less than 15  $\mu$ A each) to the differential receivers within each of the components on the AGTL+ bus. Use a voltage divider to generate a GTLREF[3:0] of  $2/3 V_{CC\_CPU} \pm 2\%$ .

**Figure 12-13. GTLREF Divider**



R1 and R2 should be small enough values that the current drawn by the GTLREF inputs ( $I_{REF}$ ) is negligible versus the current through R2 and R1. Equation 12-1 shows GTLREF, where “n” is the number of  $I_{REF}$  inputs supplied by the divider.

**Equation 12-1. GTLREF**

$$GTLREF = \frac{V_{CC}/R_2 - n \times I_{REF}}{1/R_2 + 1/R_1}$$

The worst case GTLREF should be analyzed with  $I_{REF}$  at the maximum and minimum values determined for the number of loads being supplied. If the number of loads can change from model to model because of upgrades, this should be taken into account as well. Analyze Equation 12-1 with R1 and R2 at the extremes of their tolerance specifications.

Use two voltage dividers for each processor, and one for the chipset component. Assume a maximum of 15 mA of leakage current per load. These leakage currents can be positive or negative.

The following discussion illustrates using a single voltage divider to support two GTLREF Loads assuming VCC\_CPU of 1.475 V. Using a  $100\ \Omega \pm 1\%$  resistor for R1 and a  $49.9\ \Omega \pm 1\%$  resistor for R2 in Figure 12-14 creates a static usage of  $10.7\ \mu\text{A}$  ( $1.475\ \text{V}/149.9\ \Omega$ ) per voltage divider. The worst case solution for Equation 12-1 can be found with IREF at  $30\ \mu\text{A}$ , R1 at the low end of its tolerance specification ( $99\ \Omega$ ), and R2 at the high end of its tolerance specification ( $50.4\ \Omega$ ), yielding Equation 12-2. The target of  $2/3$  of VCC\_CPU is 1.133 V. This resistive setting is within 0.7% of the  $2/3$  point and satisfies the 2% specification.

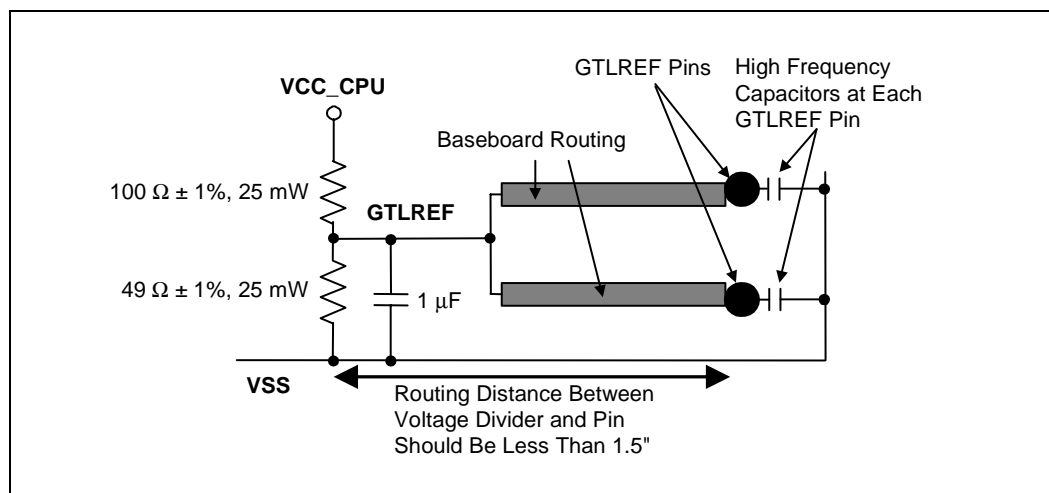
#### Equation 12-2. Resistor Tolerance Analysis

$$V_{REF} = \frac{1.475/50.4 - .000030}{1/50.4 + 1/99} = 1.1255\text{V}$$

Decouple GTLREF[3:0] at each pin with a 220 pF capacitor to VSS. Decoupling GTLREF to VSS at the voltage dividers with a  $1\ \mu\text{F}$  capacitor may further enhance the ability for GTLREF to track VCC.

When routing GTLREF to the pins, use a 30–50 mil trace (the wider the better), and keep it as short as possible (less than 1.5 inches). Also, keep all other signals at least 20 mils away from the GTLREF trace. This provides a low impedance line without the cost of an additional plane or island. Because of the placement of the GTLREF pins on the processor, it may not be possible or convenient to route all four pins from one voltage divider. It is acceptable to use more than one voltage divider with decoupling at each voltage divider and each pin.

Figure 12-14. Suggested GTLREF Generation





### 12.2.11 Component Models

Acquire component models from their respective manufacturers. Intel cannot guarantee the specifications of other manufacturers' components. This section contains some of the models developed by Intel for internal simulations.

**Table 12-7. Various Component Models Used at Intel (Not Vendor Specifications)**

Component of Simulation	ESR ( $\Omega$ )	ESL (nH)
0.1 $\mu$ F Ceramic 0603 package	0.006	0.63
1 $\mu$ F Ceramic 0805 package	0.080	0.702
10.0 $\mu$ F Ceramic 1206 package	0.010	0.880
22.0 $\mu$ F Ceramic 1210 package	0.010	0.880
560 $\mu$ F OS-CONS	0.012	2.7

### 12.2.12 Measuring Transients

Intel recommends the following guidelines when measuring the transients on VCC\_CPU. The measurement should be performed across the VCC\_CPU and VSS pins on the processor socket. Use an oscilloscope with 500 MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M $\Omega$  minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure that external noise from the system is not coupled on the scope probe. Some probes have a very significant level of inherent noise. Attempt to minimize noise by investigating different probes. Use a differential probe to make the voltage measurements. The bandwidth of the probe should be no less than that of the oscilloscope. Ensure all connections from oscilloscope to motherboard pin are good and have a very low contact resistance.

## 12.3 MCH Power Delivery Guidelines

The following guidelines are recommended for an optimal MCH power delivery. The main focus of these guidelines is to minimize chipset power noise and signal integrity problems. The guidelines are not intended to replace thorough system validation of products.

### 12.3.1 DDR\_VTT (1.25 V) Decoupling

To reduce noise on the DDR termination voltage (1.25V) around the MCH, two 0.1  $\mu$ F and two 0.01  $\mu$ F capacitors per channel are recommended. Evenly distribute placement of decoupling capacitors along the VTT plane around the MCH within 1 inch of the outer row of balls. Ceramic 0603 body type capacitors are recommended.

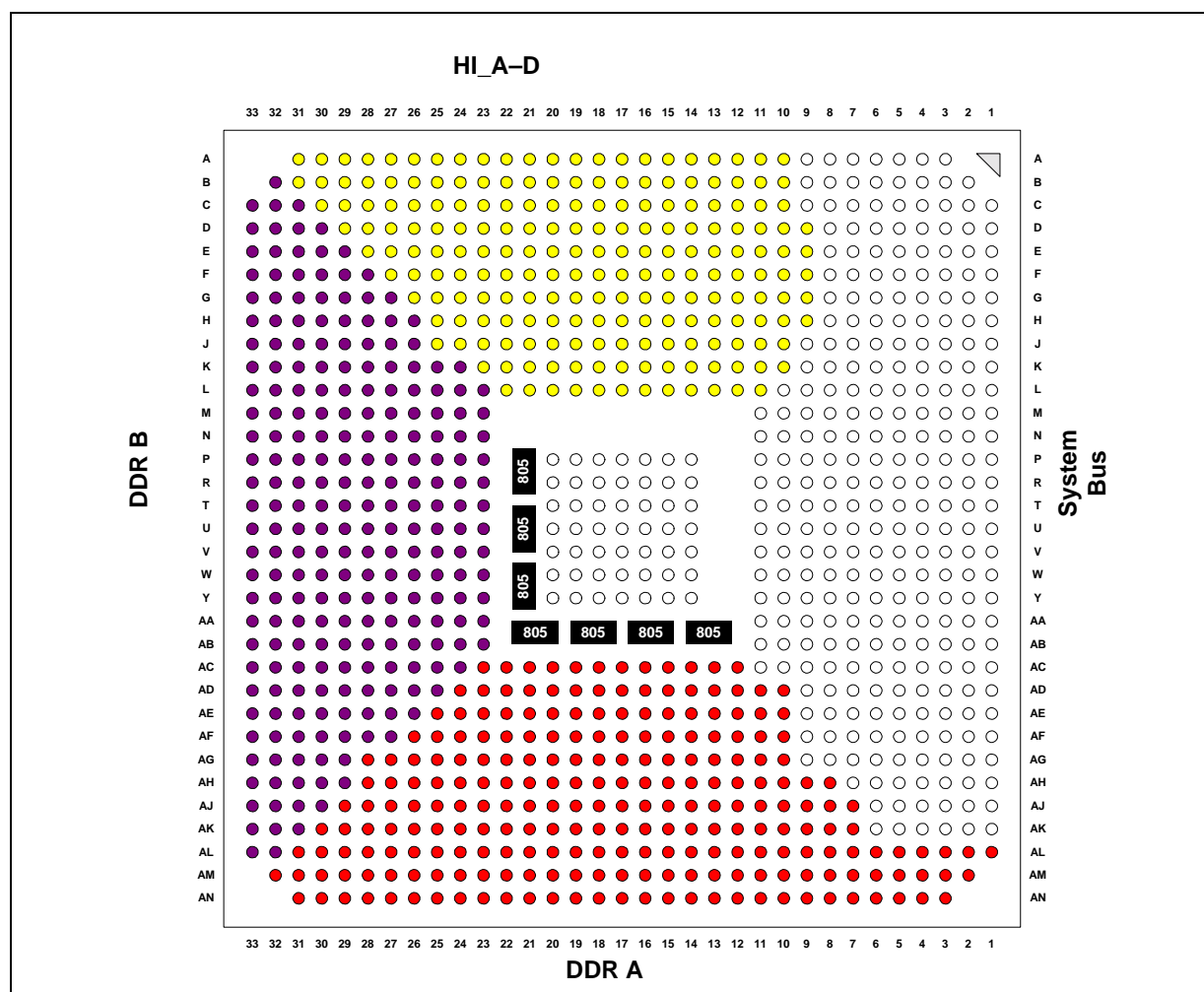
### 12.3.2 VCC\_CPU (1.45 V Power Plane)

A maximum of five, 0.1  $\mu$ F capacitors (minimum of four) are recommended (with 900 pH to 1.1 nH inductance) to be placed under the MCH for System Bus 1.50 V power plane decoupling. The designer should evenly distribute placement of decoupling capacitors among the System Bus interface signal field. In addition to the minimum decoupling capacitors under the MCH, the designer should place a maximum of nine (9) evenly spaced capacitors for the System Bus, at least seven (7) of which must be within 0.5 inch of the outer row of balls to the MCH.

### 12.3.3 DDR (2.5 V Power Plane)

A maximum of seven 0.1  $\mu$ F (minimum of five) capacitors are recommended (with 900 pH to 1.1 nH inductance) to be placed under the MCH for DDR 2.5 V power plane decoupling (see Figure 12-15). The designer should evenly distribute placement of decoupling capacitors among the DDR interface signal field. It is recommended that the designer use ceramic capacitor 0402 or 0805 body type. In addition to the minimum decoupling capacitors under the MCH, the designer should place a maximum of fifteen (15) evenly spaced capacitors for both DDR channels, and at least ten must be within 0.5 inch of the outer row of balls to the MCH.

Figure 12-15. MCH Decoupling (Backside View)



### 12.3.4 Hub Interface (1.2 V Power Plane)

A maximum of four, 0.1  $\mu$ F capacitors should be used to improve I/O power delivery to the MCH. These capacitors should be placed within 150 mils of the MCH package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1.2 side of the capacitors to the VCC1.2 power pins. Similarly, if layout allows, metal fingers running on the VCC1.2 side of the board should connect the ground side of the capacitors to the VSS power pins.

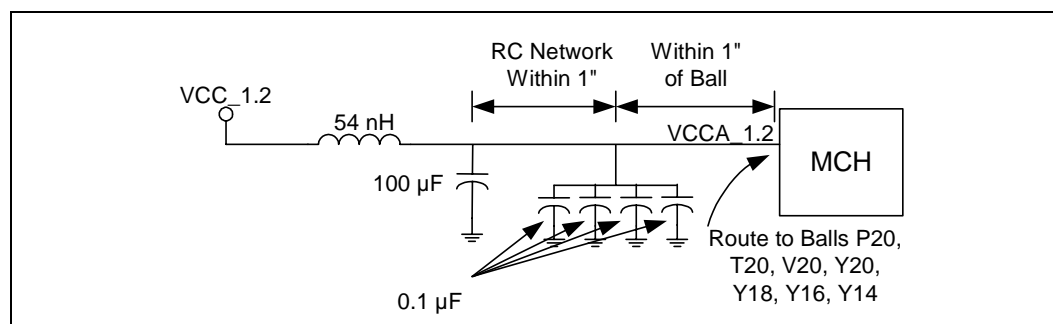
### 12.3.5 Filter Specifications (1.2V Power Plane)

VCCA\_1.2 and VCCAHI\_1.2 are created by using a low pass filter on VCC\_1.2. VCCACPU is created by using a low pass filter on VCC\_CPU. The MCH has internal analog PLL clock generators, which require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency).

When designing the VCCA\_1.2 filter (Figure 12-16), follow these guidelines:

- One 54 nH Inductor close to the edge of the package (within 1" of the die).
- One 100  $\mu$ F or 150  $\mu$ F LF capacitor close to the edge of the package.
- Minimum of two (four preferred) Low ESL HF capacitors, 0.22  $\mu$ F or 0.1  $\mu$ F, on the backside of the motherboard under the die.
- Route the VCCA\_1.2 trace 1 inch, 35 mils wide with 15 mils spacing on three signal layers of the motherboard; connect to VCCA\_1.2 island on signal layers directly under the MCH core.

**Figure 12-16. Filter Topology for VCCA\_1.2 (DDR Interface)**



When designing the VCCA\_1.2 and VCCACPU filters (Figure 12-17 and Figure 12-18), follow these guidelines:

- One 100 nH Inductor close to the edge of the package (within 1 inch of the die).
- One 100  $\mu$ F or 150  $\mu$ F LF capacitor close to the edge of the package.
- Minimum of one Low ESL HF capacitor, 0.1  $\mu$ F on the motherboard backside, under the die.

**Figure 12-17. Filter Topology for VCCAHI\_1.2 (HUB Interface)**

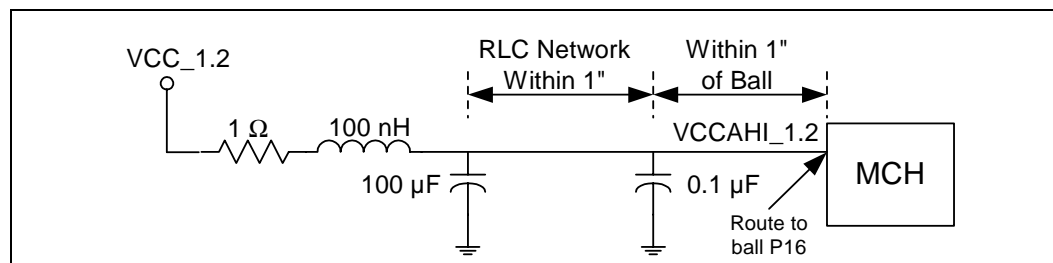
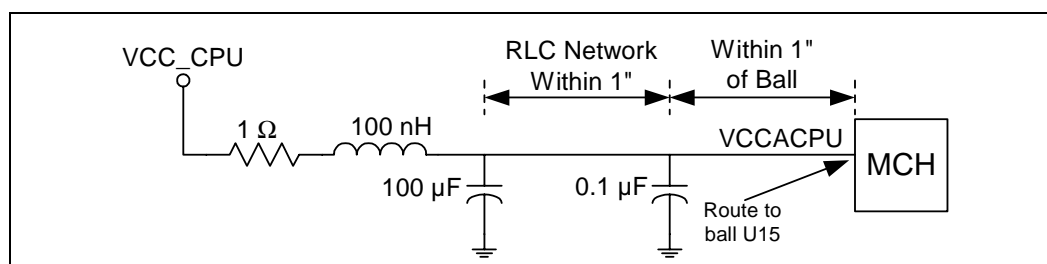


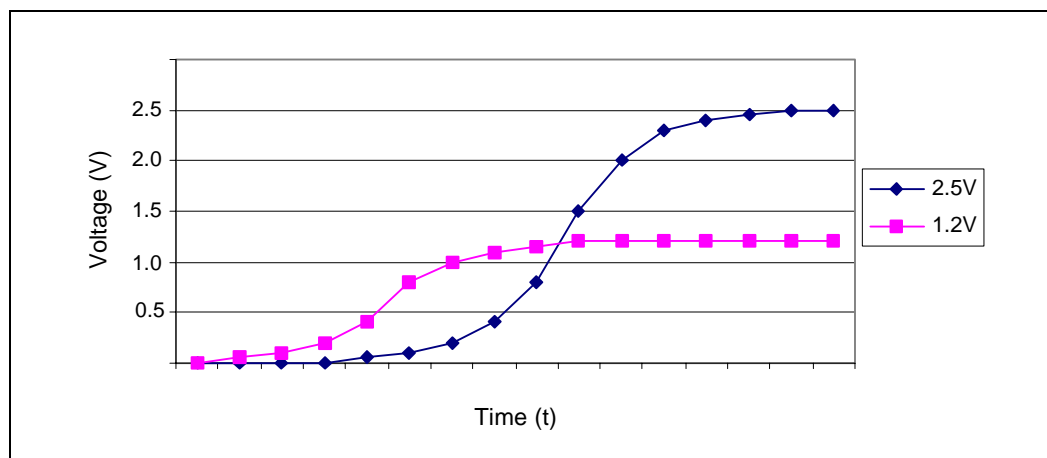
Figure 12-18. Filter Topology for VCCAHL\_1.2 (System Bus)



### 12.3.6 MCH Power Sequencing Requirement

The MCH has only one power sequencing requirement. The MCH requires that 1.2 V rises with or before 2.5 V to avoid electrical overstress of oxide layers and possible component damage. This means that at any point during system power up, the 2.5 V power plane voltage must not be higher than the 1.2 V power plane voltage until the 1.2 V voltage is within 1.2 V regulation. This is depicted in Figure 12-19. Notice that at no point before 1.2 V is ramped does the 2.5 V plane exceed the 1.2 V plane's value.

Figure 12-19. Power Sequencing Requirement for MCH

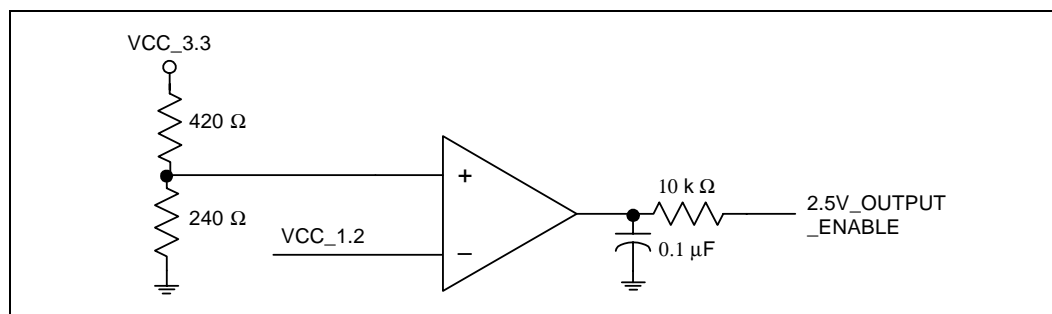


**NOTE:** This graph does not represent specific values or requirements on data/time frames.

A possible solution to safeguard against 2.5 V coming up before 1.2 V, is to tie the power good signal of the 1.2 V regulator to the output enable pin of the 2.5 V voltage regulator.

If the same voltage regulator is used to derive both 1.2 V and 2.5 V, then other logic must be used. A solution is to use a comparator to 1.2 V, and connect the output of the comparator to the output enable signal of the 2.5 V regulator. Figure 12-20 shows this implementation.

Figure 12-20. Sample 2.5 V Output Enable Control Logic



## 12.4 Intel® ICH3-S Power Delivery Guidelines

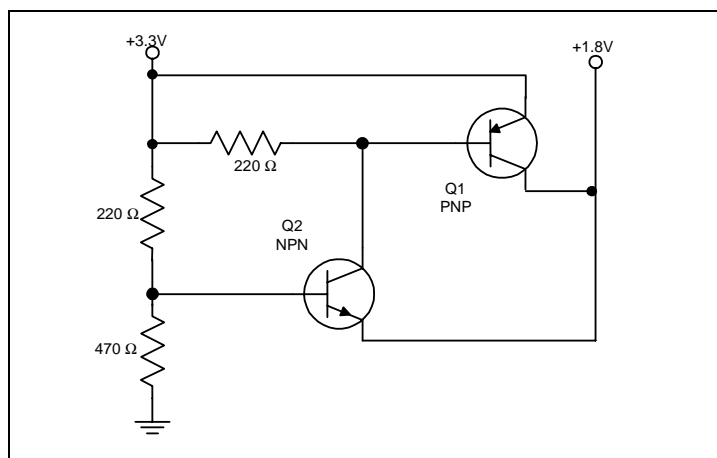
### 12.4.1 1.8 V/3.3 V Power Sequencing

The ICH3-S has two pairs of associated 1.8 V and 3.3 V supplies. These are {VCC\_1.8, VCC\_3.3} and {VCCSUS\_1.8, VCCSUS\_3.3}. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this generally does not occur because the 1.8 V supply is typically derived from the 3.3 V supply with a linear regulator). One serious consequence of violation of this “2 V Rule” is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH3-S I/O buffers are driven by the 3.3 V supplies but are controlled by logic powered by the 1.8 V supplies. Therefore, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case, the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as “Input-only” actually have output buffers that are normally disabled, and the ICH3-S may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

Figure 12-21 is an example of power-on sequencing circuit that ensures the 2 V Rule is obeyed. This circuit uses an NPN (Q2) and a PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

**Note:** Note that such circuit is not needed if the voltage regulator guarantees the 2 V Rule.

**Figure 12-21. Example 1.8 V/3.3 V Power Sequencing Circuit**

When analyzing systems that may be “marginally compliant” to the 2 V Rule, attention must be paid to the behavior of the ICH3-S’s RSMRST# and PWROK signals because they control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the resume wells.
- PWROK controls isolation between the resume wells and main wells.

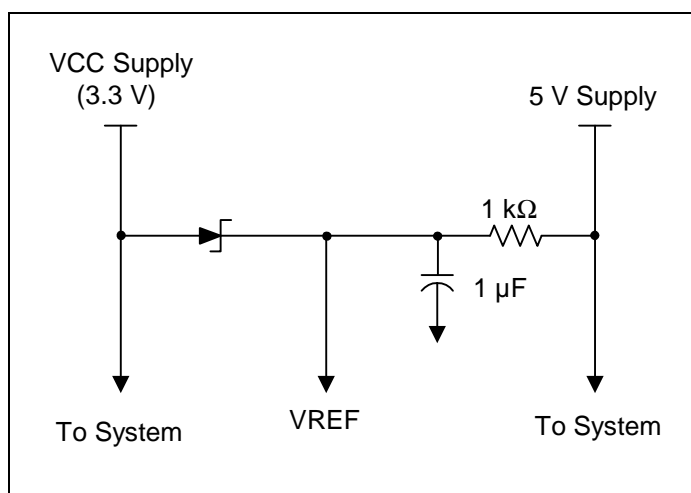
If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

## 12.4.2 3.3V/V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH3-S. V5REF must be powered up before VCC3\_3, or after VCC3\_3 within 0.7 V. Also, V5REF must power down after VCC3\_3, or before VCC3\_3 within 0.7 V. The rule must be followed in order to ensure the safety of the ICH3-S. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3\_3 rail. [Table 12-22](#) shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the standby rails, but in most platforms, the VCCSUS3\_3 rail is derived from the VCCSUS5 rail and therefore, the VCCSUS3\_3 rail will always come up after the VCCSUS5 rail. As a result, V5REF\_SUS will always be powered up before VCCSUS3\_3. In platforms that do not derive the VCCSUS3\_3 rail from the VCCSUS5 rail, this rule must be enforced on the platform.

Figure 12-22. Example 3.3 V/V5REF Sequencing Circuitry



## 12.4.3 Intel® ICH3-S Power Rails

The ICH3-S refers to its standby rails as suspend. [Table 12-8](#) lists the nomenclature.

Table 12-8. ICH3-S Power Rail Terminology

Platform Terminology	ICH3-S Terminology
5 V Standby	5 V Suspend
3.3 V Standby	3.3 V Suspend
1.8 V Standby	1.8 V Suspend

## 12.4.4 Intel® ICH3-S Decoupling Recommendations

The ICH3-S is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the decoupling capacitors specified in [Table 12-9](#) to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (200 mils nominal). It is recommended that for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Table 12-9. Intel® ICH3-S Decoupling Recommendations

Power	Decoupling Requirements	Decoupling Placement
V_CPU_IO	Use <b>one</b> 0.1 $\mu$ F decoupling capacitor.	<ul style="list-style-type: none"> <li>• Locate within 100 mils of the ICH3-S processor interface balls.</li> </ul>
VCCRTC	Use <b>one</b> 1.0 $\mu$ F decoupling capacitor. See Figure 9-10 for the External Circuitry.	<ul style="list-style-type: none"> <li>• Locate within 100 mils of the VCCRTC interface ball (ball AB6).</li> </ul>
VCC_3.3	Requires <b>six</b> 0.1 $\mu$ F decoupling capacitors.	<ul style="list-style-type: none"> <li>• Distribute around the ICH3-S package sides within 100 mils of the package balls: <ul style="list-style-type: none"> <li>– Top near AUX/PCI</li> <li>– Left across the PCI and LPC</li> <li>– Bottom near IDE</li> <li>– Right near GPIO[43]</li> </ul> </li> </ul>
VCCSUS_3.3	Requires <b>two</b> 0.1 $\mu$ F decoupling capacitors.	<ul style="list-style-type: none"> <li>• Place one capacitor on the top side within 200 mils of the USB center.</li> <li>• Place one capacitor on the bottom side near the VCCSUS_3.3 supply.</li> </ul>
VCC_1.8	Requires <b>four</b> 0.1 $\mu$ F decoupling capacitors.	<ul style="list-style-type: none"> <li>• Locate 2 capacitors distributed local to the hub interface, within 50 mils of the package HI balls.</li> <li>• Distribute the remaining capacitors on the left and bottom sides of the package for core delivery.</li> </ul>
VCCSUS_1.8	Requires <b>one</b> 0.1 $\mu$ F decoupling capacitor.	<ul style="list-style-type: none"> <li>• Locate within 200 mils of the ICH3-S, Balls B23 and C23.</li> </ul>
5VREF_SUS	Requires <b>one</b> 0.1 $\mu$ F decoupling capacitor. V5REF_SUS is the reference voltage for some 5 V tolerant inputs in the ICH3-S (USB data and over current signals). V5REF_SUS must power up before or simultaneous to VCCSUS_3.3. It must power down after or simultaneous to VCCSUS_3.3. (For most platforms, this power sequencing is not an issue as VCCSUS_3.3 is derived from 5VREF_SUS.)	
V5_REF	Requires <b>one</b> 0.1 $\mu$ F decoupling capacitor. V5_REF is the reference voltage for most 5 V tolerant inputs in the ICH3-S. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC_3.3. It must power down after or simultaneous to VCC_3.3.	



## 12.5 Intel® P64H2 Power Requirements

### 12.5.1 Intel® P64H2 Current Requirements

**Table 12-10. Intel® P64H2 Max Sustained Currents**

Voltage at PCI/PCI-X Interface	Max Sustained Current
1.8V at 33 MHz PCI (both segments)	1970 mA
1.8V at 66 MHz PCI/PCI-X (both segments)	2170 mA
1.8V at 100 MHz PCI-X (both segments)	2550 mA
1.8V at 133 MHz PCI-X (both segments)	2660 mA
3.3V at 33 MHz PCI 6 loads (both segments)	930 mA
3.3V at 66 MHz PCI 2 loads (both segments)	690 mA
3.3V at 66 MHz PCI-X 4 loads (both segments)	1300 mA
3.3V at 100 MHz PCI-X 2 loads (both segments)	1050 mA
3.3V at 133 MHz PCI-X 1 load (both segments)	770 mA

For more information, refer to the P64H2 Thermal Design Guide.

### 12.5.2 Intel® P64H2 Decoupling Requirements

The P64H2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in the table below to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible.

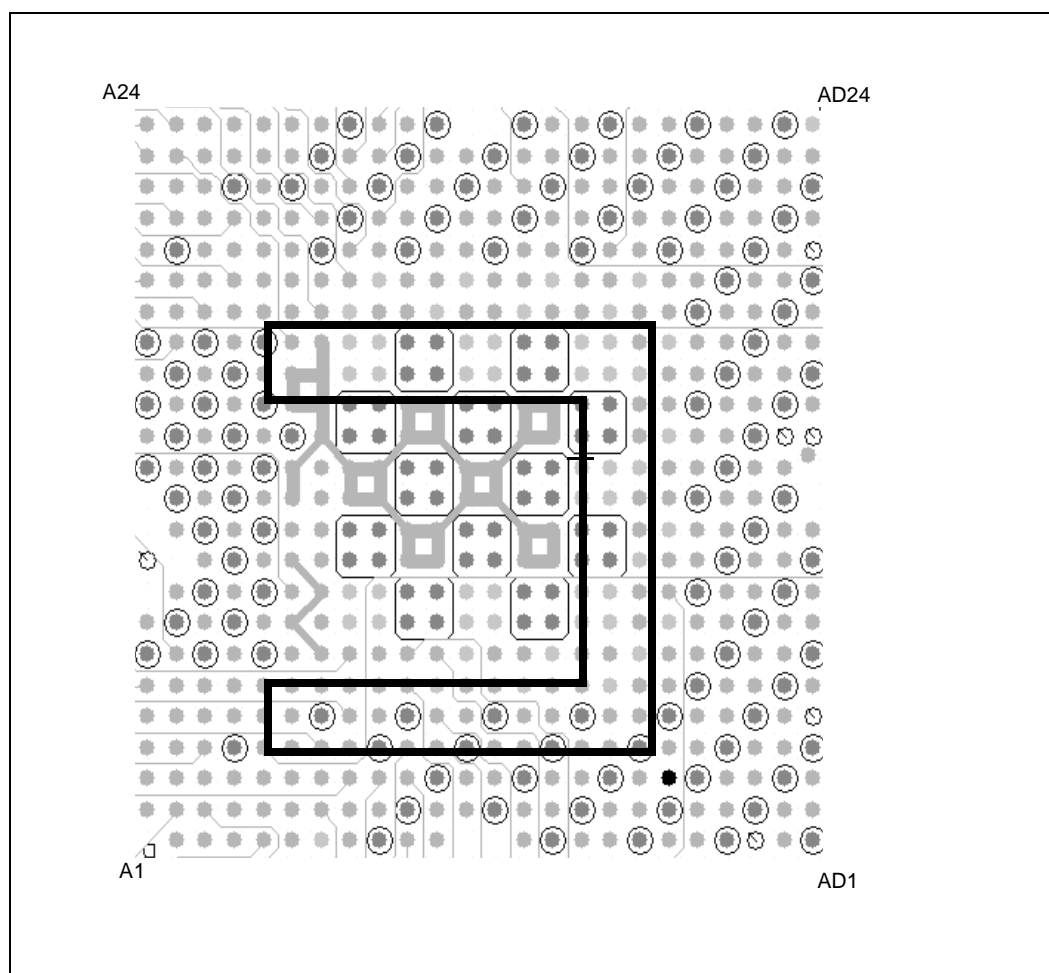
**Table 12-11. Decoupling Capacitor Recommendations**

Power Plane/Pins	Number of High-Frequency Decoupling Capacitors	High-Frequency Capacitor Values	Number of Bulk Decoupling Capacitors	Bulk Capacitor Values
1.8V Core (VCC)	8	0.1 $\mu$ F	2	4 $\mu$ F (near P64H2)
1.8V HI 2.0 (VCC_1.8)	2	1.0 $\mu$ F	1	100 $\mu$ F (near regulator)
3.3V PCI/PCI-X (VCC_3.3)	20 <sup>1</sup>	0.1 $\mu$ F	2	4 $\mu$ F (near P64H2)
	6	1.0 $\mu$ F	1	100 $\mu$ F (near regulator)

**NOTES:**

1. In the case of the 20 0.1  $\mu$ F decoupling capacitors for the Vcc3.3V plane, it is recommended that at least five of these capacitors be placed near the die on the back of the board between ground and the VCC-PCI vias, as shown in [Figure 12-23](#). This is not a strict requirement, but is recommended to reduce the power resonance frequency at 66Hz.

Figure 12-23. 3.3V PCI/PCI-X (VCC\_3.3) Capacitor Placement



**NOTE:** The outlined area in the figure is the 3.3 V plane. Place at least five 0.1  $\mu$ F capacitors in this area.

### 12.5.3 PCIRST# Implementation

PCI-X requires a 100 ms delay from valid power (PWRGD) to reset deassertion (PCIRST#). The system design must ensure this requirement is met.

The P64H2 reset must be deasserted within 60 ns of the MCH reset deassertion. Intel strongly recommends the customer to measure this timing relationship on their board. Failure to meet this guideline may result in a system failing to boot.

### 12.5.4 P64H2 Power Sequencing Requirement

3.3 V and 1.8 V must be valid before the first CLK66 pulse is drive to the P64H2. This can be guaranteed by gating the CK408 cocks using a power good signal from the 1.8 V regulator.

# Schematic Checklist

# 13

## 13.1 Processor Schematic Checklist

Table 13-1. Processor Schematic Checklist (Sheet 1 of 6)

Checklist Items	Recommendations	Comments
A20M#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Asynchronous GTL+ Input Signal.</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>
A[35:3]# <sup>1</sup>	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Source Synchronous I/O.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
ADS#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted to indicate the validity of the transaction address on the A[35:3]#<sup>1</sup> pins.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
ADSTB[1:0]# <sup>2</sup>	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Address strobes used to latch A[35:3]#<sup>1</sup> on rising and falling edge.</li> <li>AGTL+ Strobes.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
AP[1:0]#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
BCLK[1:0]	<ul style="list-style-type: none"> <li>Connect to a <math>49.9\ \Omega</math> 1% pull-down and to a series resistor (<math>20 - 33\ \Omega</math>). Connect other side of series resistor to CK-408.</li> </ul>	<ul style="list-style-type: none"> <li>All processor system bus agents must receive these signals to drive their outputs and latch their inputs.</li> <li>System Bus Clock.</li> <li>Refer to <a href="#">Section 4.1.1</a>.</li> <li><b>NOTE:</b> BCLK[1:0] are processor pin names that are connected to clocks in the Host_CLK clock group on CK408B.</li> </ul>
BINIT#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> <li>Wired-OR signal: Route as common clock signal.</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
BNR#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> <li>Wired-OR signal: Route as common clock signal.</li> </ul>	<ul style="list-style-type: none"> <li>Used to assert a bus stall by any bus agent who is unable to accept new bus transactions.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
BPM[5:0]#		<ul style="list-style-type: none"> <li>AGTL+ Common Clock I/O.</li> <li>For all ITP interface signal schematic, layout and routing recommendations, refer to the <i>ITP700 Debug Port Design Guide</i>.</li> </ul>

Table 13-1. Processor Schematic Checklist (Sheet 2 of 6)

Checklist Items	Recommendations	Comments
BPRI#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Used to arbitrate for ownership of the processor system bus.</li> <li>AGTL+ Common Clock Input.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
BR[3:0]#	<ul style="list-style-type: none"> <li>Connect BR[0]# to the MCH's BREQ0# pin, Processor 0's BR0# pin, and Processor 1's BR1# pin. Terminate using a <math>50\ \Omega \pm 5\%</math> pull-up resistor at Processor 0.</li> <li>Connect BR[1]# signal to Processor 0's BR1# pin and Processor 1's BR0# pin. Terminate both ends of the bus using <math>50\ \Omega \pm 5\%</math> pull-up resistors.</li> <li>BR[3:2]# should be terminated individually at each processor or be connected between processors and terminated at one end using a <math>50\ \Omega \pm 5\%</math> pull-up resistor.</li> <li>Refer to <a href="#">Figure 5-10</a> for more clarification.</li> </ul>	<ul style="list-style-type: none"> <li>Used to arbitrate for ownership of the processor system bus.</li> <li>These signals do not have on-die processor termination and must be terminated on the motherboard.</li> <li>BR0# is an AGTL+ Common Clock I/O.</li> <li>BR[3:1]# are AGTL+ Common Clock Inputs.</li> <li>Refer to <a href="#">Section 5.3.6</a>.</li> </ul>
COMP[1:0]	<ul style="list-style-type: none"> <li>Terminate to ground separately using <math>50\ \Omega \pm 1\%</math>.</li> </ul>	<ul style="list-style-type: none"> <li>Power/Other.</li> <li>Sets the processor's on-die termination.</li> <li>Refer to <a href="#">Section 5.3.5</a>.</li> </ul>
D[63:0]# <sup>3</sup>	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Source Synchronous I/O.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
DBI[3:0]#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Indicates the polarity of the D[63:0]#<sup>3</sup> signals.</li> <li>AGTL+ Source Synchronous I/O.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
DBSY#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
DEFER#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion.</li> <li>AGTL+ Common Clock Input.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
DP[3:0]#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Provides parity protection for the D[63:0]#<sup>3</sup> signals.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
DRDY#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by data driver on each data transfer to indicate valid data.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>

**Table 13-1. Processor Schematic Checklist (Sheet 3 of 6)**

Checklist Items	Recommendations	Comments
DSTBN[3:0]# <sup>4</sup> DSTBP[3:0]# <sup>5</sup>	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Data strobe used to latch in D[63:0]#<sup>3</sup>.</li> <li>Maintain a 25 mil spacing from other signals.</li> <li>AGTL+ Strobes.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
FERR#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Pull-up at both ends of the signal with <math>56\ \Omega \pm 5\%</math> to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by processor to indicate floating-point error.</li> <li>Async. GTL+.</li> <li>Refer to <a href="#">Section 5.3.1</a>.</li> </ul>
HIT#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> <li>Wired-OR signal: Route as common clock signal.</li> </ul>	<ul style="list-style-type: none"> <li>Convey transaction snoop operation results.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
HITM#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> <li>Wired-OR signal: route as common clock signal.</li> </ul>	<ul style="list-style-type: none"> <li>Convey transaction snoop operation results.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
HLOCK# (LOCK#)	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Indicates to the system that a transaction must occur atomically.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
IERR#	<ul style="list-style-type: none"> <li>If supported, connect to both processors and the ICH3-S. Terminate at both ends with <math>56\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> <li>If not supported, leave as no-connect or connect to a Baseboard Management Controller (BMC).</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by the processor to indicate an internal error.</li> <li>Asynchronous GTL+ Output.</li> <li>Refer to <a href="#">Section 5.3.1</a>.</li> </ul>
IGNNE#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted to processor to ignore numeric error.</li> <li>Asynchronous GTL+ Input.</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>
INIT#	<ul style="list-style-type: none"> <li>Connect to both processors, FWH and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> <li>Voltage translator circuit is required for FWH.</li> </ul>	<ul style="list-style-type: none"> <li>Resets processor internal registers without affecting internal caches. Also used to enable BIST.</li> <li>Asynchronous GTL+ Input.</li> <li>Refer to <a href="#">Section 5.3.2.2</a>.</li> </ul>
LINT1 LINT0	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Used as local APIC interrupts when APIC is enabled.</li> <li>Map to INTR and NMI in ICH3-S.</li> <li>Asynchronous GTL+ Input.</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>
MCERR#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> <li>Wired-OR signal: Route as common clock signal.</li> </ul>	<ul style="list-style-type: none"> <li>Convey transaction snoop operation results.</li> <li>AGTL+ Common Clock I/O.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>

Table 13-1. Processor Schematic Checklist (Sheet 4 of 6)

Checklist Items	Recommendations	Comments
ODTEN	<ul style="list-style-type: none"> <li>Enable on-die termination (ODT) on Processor 0 (end processor) by pulling up to VCC_CPU with a <math>50\ \Omega \pm 20\%</math> resistor.</li> <li>Disable ODT for Processor 1 by pulling down to V<sub>SS</sub> with a <math>50\ \Omega \pm 20\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Enables processor on-die termination.</li> <li>Input.</li> <li>Refer to <a href="#">Section 5.3.7</a>.</li> </ul>
PROCHOT#	<ul style="list-style-type: none"> <li>Pull-up at both ends of PROCHOT# with a <math>56\ \Omega \pm 5\%</math> to VCC_CPU.</li> <li>Connect to both processors and ICH3-S GPIO or a baseboard management controller (BMC) if implemented in the platform. A BMC can connect individually to each processor in order to determine which processor asserted PROCHOT#.</li> </ul>	<ul style="list-style-type: none"> <li>Indicates the processor Thermal Control Circuit has been activated.</li> <li>Asynchronous GTL+ Output.</li> <li>Refer to <a href="#">Section 5.3.1</a>.</li> </ul>
PWRGOOD (CPUPWRGOOD)	<ul style="list-style-type: none"> <li>Recommend <math>300\ \Omega \pm 5\%</math> pull-up to VCC_CPU. Connect to both processors and ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Asynchronous GTL+ Input.</li> <li>Asserted by ICH3-S when all processor voltage supplies are stable.</li> <li>Refer to <a href="#">Section 5.3.2.1</a>.</li> </ul>
REQ[4:0]# <sup>6</sup>	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by current bus owner to define the currently active transaction type.</li> <li>AGTL+ Source Synchronous I/O.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
Reserved	<ul style="list-style-type: none"> <li>Reserved signals must remain as No Connect (NC).</li> </ul>	
RESET# <sup>7</sup>	<ul style="list-style-type: none"> <li>Recommend <math>51\ \Omega \pm 5\%</math> pull-up to VCC_CPU. Connect to MCH and both processors. Note that this signal is dual terminated at both ends of transmission line.</li> </ul>	<ul style="list-style-type: none"> <li>Resets all processors to known states and invalidates caches without writing back their contents.</li> <li>AGTL+ Common Clock Input.</li> <li>Refer to <a href="#">Section 5.2.2</a>.</li> <li>If using ITP, for signal connection to ITP, refer to the <i>ITP700 Debug Port Design Guide</i> for all schematic, layout and routing recommendations.</li> </ul>
RS[2:0]#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Driven by response agent.</li> <li>AGTL+ Common Clock Input.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
RSP#	<ul style="list-style-type: none"> <li>Connect to both processors and the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Provides parity for RS[2:0]# signals.</li> <li>AGTL+ Common Clock Input.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
SKTOCC#	<ul style="list-style-type: none"> <li>If supported, pull-up to VCC_3.3; otherwise leave as NC.</li> </ul>	<ul style="list-style-type: none"> <li>Power/Other</li> <li>Output of this signal indicates whether a processor is installed or not; prevents powering up the voltage regulators for the processors.</li> <li>Refer to <a href="#">Section 5.3.9</a>.</li> </ul>

Table 13-1. Processor Schematic Checklist (Sheet 5 of 6)

Checklist Items	Recommendations	Comments
SLP# (CPUSLP#)	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Causes processor to enter sleep state.</li> <li>Asynchronous GTL+ Input.</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>
SM_ALERT#	<ul style="list-style-type: none"> <li>Should be connected to the SMBus controller.</li> </ul>	<ul style="list-style-type: none"> <li>SMBus I/O.</li> <li>Refer to <a href="#">Section 5.3.4</a>.</li> </ul>
SM_CLK SM_DAT	<ul style="list-style-type: none"> <li>Connect to both processors and SMBus controller.</li> <li>Recommend a pull-up resistor to VCC_3.3. Resistor value is based on the number of devices on the SMBus.</li> </ul>	<ul style="list-style-type: none"> <li>SMBus Input.</li> <li>Refer to <a href="#">Section 5.3.4</a>.</li> </ul>
SM_EP_A[2:0]	<ul style="list-style-type: none"> <li>Leave as no connect to set bit low, or pull-up to SM_VCC through <math>100\ \Omega \pm 5\%</math> resistor to set bit high.</li> <li>Use these address bits to set a unique SMBus address for the memory devices on the processor. See the <i>Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet</i> for more details.</li> </ul>	<ul style="list-style-type: none"> <li>Set the SMBus address for the memory device on the processor. These signals must be set at power up with a unique address per bus.</li> <li>These signals have <math>10\ \text{k}\Omega</math> pull-downs on the processor.</li> <li>SMBus Input.</li> <li>Refer to <a href="#">Section 5.3.4</a>.</li> </ul>
SM_TS_A[1:0]	<ul style="list-style-type: none"> <li>Leave as no connect to set bit to high-impedance state. Pull-up to SM_VCC through <math>1\ \text{k}\Omega \pm 5\%</math> to set bit high. Pull-down to VSS through <math>1\ \text{k}\Omega \pm 5\%</math> to set bit low. Use these address bits to set a unique SMBus address for the thermal devices on the processor. See the <i>Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz Datasheet</i> for more details.</li> </ul>	<ul style="list-style-type: none"> <li>These signals do not have internal pull-downs. Leaving the pins floating causes a high impedance state.</li> <li>SMBus Input.</li> <li>Refer to <a href="#">Section 5.3.4</a>.</li> </ul>
SM_VCC	<ul style="list-style-type: none"> <li>Connect to 3.3 V power supply.</li> </ul>	
SM_WP	<ul style="list-style-type: none"> <li>Pull to VCC_SMBus with <math>100\ \Omega \pm 5\%</math> resistor to write-protect the processor's Scratch EEPROM. Leave as no connect (NC) to disable write-protecting of Scratch EEPROM.</li> </ul>	<ul style="list-style-type: none"> <li>Pulling this signal to VCC_SMBus enables write protection on the processor scratchpad memory device.</li> <li>SMBus Input.</li> <li>Refer to <a href="#">Section 5.3.4</a>.</li> </ul>
SMI#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted asynchronously by system logic.</li> <li>Asynchronous GTL+ Input</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>
STPCLK#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S. Include <math>200\ \Omega \pm 5\%</math> pull-up to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Causes processors to enter a low power Stop-grant state.</li> <li>Asynchronous GTL+ Input.</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>

Table 13-1. Processor Schematic Checklist (Sheet 6 of 6)

Checklist Items	Recommendations	Comments
TESTHI[6:0]	<ul style="list-style-type: none"> <li>Option 1: Recommend separate <math>50\ \Omega \pm 20\%</math> pull-up to VCC_CPU.</li> <li>Option 2: TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single <math>50\ \Omega</math> resistor if desired. However, boundary scan test cannot be performed if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins.</li> </ul>	<ul style="list-style-type: none"> <li>Input.</li> <li>Refer to <a href="#">Section 5.3.8</a>.</li> </ul>
THERMTRIP#	<ul style="list-style-type: none"> <li>Connect to both processors, power control logic and, if supported, a Baseboard Management Controller (BMC). Pull-up at both ends of the signal with <math>56\ \Omega \pm 5\%</math> resistors to VCC_CPU.</li> </ul>	<ul style="list-style-type: none"> <li>Disables the VCC_CPU supply to the processors should it ever become asserted.</li> <li>Asynchronous GTL+ Output.</li> <li>Refer to <a href="#">Section 5.3.1</a>.</li> </ul>
TRDY# <sup>8</sup>	<ul style="list-style-type: none"> <li>Connect to MCH and both processors.</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Common Clock Input.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
VCCA	<ul style="list-style-type: none"> <li>Use discrete RLC filter to provide clean power.</li> </ul>	<ul style="list-style-type: none"> <li>An isolated power for internal PLL.</li> <li>Refer to <a href="#">Section 12.2.8</a>.</li> </ul>
VCCIOPLL	<ul style="list-style-type: none"> <li>Use discrete RLC filter to provide clean power.</li> </ul>	<ul style="list-style-type: none"> <li>An isolated power for internal PLL.</li> <li>Refer to <a href="#">Section 12.2.8</a>.</li> </ul>
VCCSENSE		<ul style="list-style-type: none"> <li>Isolated low impedance connection to processor core VCC_CPU.</li> <li>Refer to <a href="#">Section 12.2.3</a>.</li> </ul>
VID[4:0]	<ul style="list-style-type: none"> <li>Should be routed individually from each processor to the voltage regulator supplying its VCC_CPU supply. Refer to <i>VRM 9.1 DC-DC Converter Design Guidelines</i> for VRM details.</li> <li>Compare VIDs from both processors using glue logic to disable VR/VRM if VIDs of both processors do not match.</li> </ul>	<ul style="list-style-type: none"> <li>Processor drives these signals to indicate maximum core voltage allowed. SM_VCC must be correct and stable before the VRM should rely on these outputs.</li> </ul>
VSSA	<ul style="list-style-type: none"> <li>Use discrete RLC filter to provide clean power.</li> </ul>	<ul style="list-style-type: none"> <li>Isolated ground for internal PLLs.</li> <li>Refer to <a href="#">Section 12.2.8</a>.</li> </ul>
VSSSENSE		<ul style="list-style-type: none"> <li>An isolated low impedance connection to processor core VSS.</li> <li>Refer to <a href="#">Section 12.2.3</a>.</li> </ul>

**NOTES:**

1. A[35:3]# pins on the processor correspond to HA[35:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
4. DSTBN[3:0]# pins on the processor correspond to HADSTBN[3:0]# pins on the MCH.
5. DSTBP[3:0]# pins on the processor correspond to HADSTBP[3:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.



## 13.2 MCH Schematic Checklist

Table 13-2. MCH Schematic Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments
<b>Host Interface</b>		
ADS# AP[1:0] BINIT# BNR# BPRI# BREQ0# <sup>1</sup> CPURST# <sup>2</sup> DBI[3:0]# DBSY# DEFER# DPI[3:0]# DRDY# HA[35:3]# <sup>3</sup> HD[63:0]# <sup>4</sup> HADSTB[1:0]# <sup>5</sup> HDSTBN[3:0]# <sup>6</sup> HDSTBP[3:0]# <sup>7</sup> HIT# HITM# HLOCK# HREQ[4:0]# <sup>8</sup> HTRDY# <sup>9</sup> RS[2:0]# RSP# XERR# <sup>10</sup>	<ul style="list-style-type: none"> <li>See processor section of this checklist.</li> </ul>	
<b>DDR Interfaces A &amp; B / Connector</b>		
DQ[63:0] CB[7:0] DQS[17:0]	<ul style="list-style-type: none"> <li>Place a <math>10\ \Omega \pm 2\%</math> series resistor between MCH and first DIMM. Resistor Packs can be used. Terminate these signals to DDR VTERM (1.25 V) through a <math>22\ \Omega \pm 2\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Signal Integrity.</li> <li>Refer to <a href="#">Section 6.2</a>.</li> </ul>
MA[12:0] BA[1:0] RAS# CAS# WE#	<ul style="list-style-type: none"> <li>Terminate these signals to DDR VTERM (1.25 V) through a <math>22\ \Omega \pm 2\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.4</a>.</li> </ul>
CS[7:0]#	<ul style="list-style-type: none"> <li>Terminate these signals to DDR VTERM (1.25 V) through a <math>22\ \Omega \pm 2\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Signal Integrity.</li> <li>Refer to <a href="#">Section 6.5</a>.</li> </ul>
CMDCLK[3:0] CMDCLK[3:0]#	<ul style="list-style-type: none"> <li>Connect directly to the corresponding DIMM.</li> </ul>	<ul style="list-style-type: none"> <li>Signal Integrity.</li> <li>Refer to <a href="#">Section 6.3</a>.</li> </ul>
CKE	<ul style="list-style-type: none"> <li>Terminate CKE to DDR VTERM (1.25 V) through a <math>22\ \Omega \pm 2\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.6</a>.</li> </ul>
RCVENIN# RCVENOUT#	<ul style="list-style-type: none"> <li>Route RCVENOUT# to RCVENIN#. Place a <math>47\ \Omega \pm 2\%</math> parallel resistor to DDR VTERM as close as possible to the MCH on the RCVENIN# side. Refer to <a href="#">Figure 6-13</a>.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.7</a>.</li> </ul>
DDRCOMP	<ul style="list-style-type: none"> <li>Pull-up to DDR VTERM (1.25 V) through a <math>6.81\ \Omega \pm 1\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.8</a>.</li> </ul>
DDRCVOL DDRCVOH	<ul style="list-style-type: none"> <li>Connect as shown in <a href="#">Figure 6-15</a>.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.8</a>.</li> </ul>

Table 13-2. MCH Schematic Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments
<b>Hub Interface A</b>		
HI[11:0]	<ul style="list-style-type: none"> <li>Maximum length of 20" (stripline routing).</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.3.1</a>.</li> </ul>
HI_STBF <sup>11</sup> HI_STBS <sup>11</sup>	<ul style="list-style-type: none"> <li>Connect to ICH3-S.</li> <li>Must NOT have pull-up, pull-down, or series resistors.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.3.1</a>.</li> </ul>
<b>Hub Interface B, C, D</b>		
HI[18:0] HI[21:20]	<ul style="list-style-type: none"> <li>Maximum length of 20" (stripline routing).</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.2.1</a>.</li> </ul>
PSTRBF PSTRBS PUSTRBF PUSTRBS	<ul style="list-style-type: none"> <li>Connect to P64H2.</li> <li>Must <b>not</b> have pull-up, pull-down, or series resistors.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.2</a>.</li> </ul>
<b>Clocks, Reset, Miscellaneous Signals</b>		
HCLKINP HLCKINN	<ul style="list-style-type: none"> <li>Route with a <math>49.9\ \Omega \pm 1\%</math> pull-down resistor to ground.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.1</a>.</li> </ul>
CLK66	<ul style="list-style-type: none"> <li>Place <math>43\ \Omega</math> series resistor close to CK408B.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.2</a>.</li> </ul>
RSTIN#	<ul style="list-style-type: none"> <li>Connect to PCIRST# output of the ICH3-S.</li> </ul>	
<b>Miscellaneous Signals</b>		
XORMODE#	<ul style="list-style-type: none"> <li><math>4.7\ \text{k}\Omega \pm 5\%</math> pull-up to VCC_3.3.</li> </ul>	<ul style="list-style-type: none"> <li>Required for normal operation.</li> </ul>
Reserved (Ball B30)	<ul style="list-style-type: none"> <li><math>4.7\ \text{k}\Omega \pm 5\%</math> pull-up to VCC_3.3.</li> </ul>	<ul style="list-style-type: none"> <li>Required for normal operation.</li> </ul>
Reserved (Ball D29)	<ul style="list-style-type: none"> <li><math>1\ \text{k}\Omega \pm 5\%</math> pull-down to Ground.</li> </ul>	<ul style="list-style-type: none"> <li>Required for normal operation.</li> </ul>
HIRCOMP_A	<ul style="list-style-type: none"> <li>Tie the MCH RCOMP pin to a <math>24.9\ \Omega \pm 1\%</math> pull-up to VCC_1.2</li> <li>(For Trace Impedance = <math>50\ \Omega \pm 10\%</math>).</li> </ul>	<ul style="list-style-type: none"> <li>Used to calibrate the I/O Buffers.</li> <li>Resistive compensation is used by the ICH3-S and MCH to adjust the buffer characteristics to specific board characteristic.</li> <li>Refer to <a href="#">Section 7.3.3</a>.</li> </ul>
HIRCOMP_B HIRCOMP_C HIRCOMP_D	<ul style="list-style-type: none"> <li>Tie the MCH RCOMP pins to a <math>24.9\ \Omega \pm 1\%</math> pull-up to VCC_1.2 (For trace impedance = <math>50\ \Omega \pm 10\%</math>).</li> <li>Tie the P64H2 RCOMP pins to a <math>61.9\ \Omega \pm 1\%</math> pull-up to VCC_1.8 (For trace impedance = <math>50\ \Omega \pm 10\%</math>).</li> </ul>	<ul style="list-style-type: none"> <li>Used to calibrate the I/O Buffers.</li> <li>Resistive compensation is used by the P64H2 and MCH to adjust the buffer characteristics to specific board characteristics.</li> <li>Refer to <a href="#">Section 7.2.3</a>.</li> </ul>
HXRCOMP HYRCOMP	<ul style="list-style-type: none"> <li>Tie each COMP pin to a <math>25\ \Omega \pm 1\%</math> pull-down resistor to ground.</li> </ul>	<ul style="list-style-type: none"> <li>This signal is used to calibrate the Host AGTL+ I/O buffer characteristics to specific board characteristics.</li> <li>Refer to <a href="#">Section 5.3.5</a>.</li> </ul>

Table 13-2. MCH Schematic Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments
Unused 16 bit interfaces	<ul style="list-style-type: none"> <li>All data and strobe signals can be left as no connect.</li> <li>HIVREF_[D:A] must be connected to the reference voltage divider circuit.</li> <li>HIVSWNG_[D:A] must be connected to the reference voltage swing divider circuit.</li> <li>Leave any of the HIRCOMP_[D:A] as no connects if that hublink is not used.</li> </ul>	<ul style="list-style-type: none"> <li>The MCH has integration detection logic that will detect unpopulated 16-bit interfaces without external pull-ups and pull-downs.</li> <li>Refer to <a href="#">Section 7.2.5</a>.</li> </ul>
<b>Voltage References – Power Planes</b>		
HDVREF[3:0] HAVREF[1:0] HCCVREF	<ul style="list-style-type: none"> <li>Use one dedicated voltage divider for all these signals.</li> <li>Decouple the voltage divider with a 1 <math>\mu</math>F capacitor.</li> </ul>	<ul style="list-style-type: none"> <li>To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface.</li> <li>Refer to <a href="#">Section 12.2.10</a>.</li> </ul>
VREF_DDR[5:0]	<ul style="list-style-type: none"> <li>Decouple each signal to ground with 0.1 <math>\mu</math>F parallel capacitor at each DIMM and MCH pin.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.9</a>.</li> </ul>
HXSWING HYSWING	<ul style="list-style-type: none"> <li>The host compensation reference voltage can be implemented using a simple voltage divider circuit.</li> <li>150 <math>\Omega \pm 1\%</math> pull-down to ground</li> <li>301 <math>\Omega \pm 1\%</math> pull-up to VCC_CPU</li> <li>C1 = C2 = 0.01 <math>\mu</math>F</li> </ul>	<ul style="list-style-type: none"> <li>The HXSWING and HYSWING inputs of MCH are used to provide reference voltage for the compensation logic.</li> <li>Refer to <a href="#">Section 5.3.5</a>.</li> </ul>
HISWNG_[D:A], HIVREF[D:A]	<ul style="list-style-type: none"> <li>MCH Hub reference swing voltage = 0.800 V <math>\pm</math> 5%.</li> <li>R1 = 392 <math>\Omega \pm 1\%</math>, R2 = 499 <math>\Omega \pm 1\%</math>, R3 = 453 <math>\Omega \pm 1\%</math>.</li> <li>C1 = 0.1 <math>\mu</math>F, C2 = 0.01 <math>\mu</math>F.</li> <li>Refer to <a href="#">Figure 7-5</a> and <a href="#">Figure 7-8</a>.</li> </ul>	<ul style="list-style-type: none"> <li>The MCH 16-bit hub interfaces use a compensation voltage to control the buffer voltage characteristics. If multiple 16-bit hub interfaces are used, an HISWNG divider circuit can be shared among the interfaces as long as the trace length from the divider circuit is less than 3.5".</li> <li>Refer to <a href="#">Section 7.2.2</a> and <a href="#">Section 7.3.2</a>.</li> </ul>

**NOTES:**

1. The BREQ0# pin on the MCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the MCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the MCH correspond to A[35:3]# pins on the processor.
4. HD[63:0]# pins on the MCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the MCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the MCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the MCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the MCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the MCH corresponds to the TRDY# pin on the processor.
10. The MCH XERR# pin can be connected to the processor IERR# pin or the processor MCERR# pin.
11. In HI1.0 mode, HI\_STBF and HI\_STBS used to be referred as HI\_STB# and HI\_STB respectively.

## 13.3 Intel® ICH3-S Schematic Checklist

**Note:** There are no inputs to the ICH3-S that can be left floating.

**Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 1 of 8)**

Checklist Items	Recommendations	Comments
<b>Processor Signals</b>		
A20M# CPUSLP# (SLP#) FERR# IGNNE# INIT# LINT1 <sup>1</sup> LINT0 <sup>1</sup> SMI# STPCLK#	<ul style="list-style-type: none"> <li>Refer to the signal recommendations under the Processor Schematic Checklist.</li> </ul>	
RCIN# A20GATE	<ul style="list-style-type: none"> <li>Pull-up is required if driven by an open drain signal (the value of the resistor is determined by the driver).</li> </ul>	<ul style="list-style-type: none"> <li>Typically driven by Open Drain External Micro-controller.</li> </ul>
CPUPWRGD	<ul style="list-style-type: none"> <li>Recommend 300 <math>\Omega</math> <math>\pm</math> 5% pull-up to VCC_CPU. Connect to both processors and ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Asserted by ICH3-S when all processor voltage supplies are stable.</li> </ul>
<b>FWH Interface</b>		
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	<ul style="list-style-type: none"> <li>No extra pull-ups required. Connect straight to FWH/LPC and, if supported, a BMC.</li> </ul>	<ul style="list-style-type: none"> <li>ICH3-S Integrates 24 k<math>\Omega</math> pull-up resistors on these signal lines.</li> </ul>
<b>GPIO</b>		
GPIO[7:0]	<ul style="list-style-type: none"> <li>These pins are in the Main Power Well. Pull-ups must use the VCC_3.3 plane.</li> <li>Unused core well inputs must be pulled up to VCC_3.3.</li> <li>GPIO[1:0] can be used as REQ[B:A]#.</li> <li>GPIO[1] can be used as PCI REQ[5]#.</li> <li>GPIO[5:2] can be used as PIRQ[H:E]#.</li> <li>These signals are 5 V tolerant.</li> </ul>	<ul style="list-style-type: none"> <li>Ensure all unconnected signals are <b>outputs only</b>.</li> </ul>
GPIO[8] & [13:11]	<ul style="list-style-type: none"> <li>These pins are in the Resume Power Well. Pull-ups go to VCC_SUS3.3 plane.</li> <li>Unused resume well inputs must be pulled up to VCC_SUS3.3.</li> <li>These are the only GPIOs that can be used as ACPI compliant wake events.</li> <li>These signals are not 5 V tolerant.</li> <li>GPIO[11] can be used as SMBALERT#.</li> </ul>	<ul style="list-style-type: none"> <li>These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.</li> </ul>
GPIO[23:16]	<ul style="list-style-type: none"> <li>Fixed as output only. Can be left NC.</li> <li>In Main Power Well.</li> <li>GPIO[22] is open drain.</li> <li>GPIO[17:16] can be used as GNT[B:A]#.</li> <li>GPIO[17] can be used as PCI GNT[5]#.</li> </ul>	
GPIO[28,27,25,24]	<ul style="list-style-type: none"> <li>I/O pins. Defaults as an output. Can be left NC.</li> <li>From resume power well. (VCC_SUS3.3).</li> </ul>	

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 2 of 8)

Checklist Items	Recommendations	Comments
GPIO[43:32]	<ul style="list-style-type: none"> <li>I/O pins. Defaults as an output when enabled as GPIOs.</li> <li>From main power well (VCC_3.3).</li> </ul>	
<b>Hub Interface</b>		
HI[11]	<ul style="list-style-type: none"> <li>No pull-up resistor required.</li> </ul>	<ul style="list-style-type: none"> <li>Use a no-stuff or a test point to put the ICH3-S into NAND chain mode testing.</li> <li>Refer to <a href="#">Section 7.3.1</a>.</li> </ul>
HICOMP	<ul style="list-style-type: none"> <li>Tie the pin to a <math>78.7\ \Omega \pm 1\%</math> pull-up resistor to VCC_1.8.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.3.3</a>.</li> </ul>
HIREF	<ul style="list-style-type: none"> <li><math>0.350\ \text{V} \pm 5\%</math></li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.3.2</a>.</li> </ul>
HITERM	<ul style="list-style-type: none"> <li><math>0.700\ \text{V} \pm 5\%</math></li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.3.2</a>.</li> </ul>
<b>IDE Checklist</b>		
PDD[15:0] SDD[15:0]	<ul style="list-style-type: none"> <li>No extra series termination resistors or other pull-ups/pull-downs are required.</li> <li>PDD7/SDD7 does not require a 10 k<math>\Omega</math> pull-down resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to ATA ATAPI-6 specification. These signals have integrated series resistors.</li> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul> <p><b>NOTE:</b> Simulation data indicates that the integrated series termination resistors are a nominal 33 <math>\Omega</math>, but can range from 31 <math>\Omega</math> to 43 <math>\Omega</math>.</p>
PDIOW# PDIOR# PDDACK# PDA[2:0] PDCS1# PDCS3# SDIOW# SDIOR# SDDACK# SDA[2:0] SDCS1# SDCS3#	<ul style="list-style-type: none"> <li>No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.</li> </ul>	<ul style="list-style-type: none"> <li>These signals have integrated series resistors.</li> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul> <p><b>NOTE:</b> Simulation data indicates that the integrated series termination resistors are a nominal 33 <math>\Omega</math>, but can range from 31 <math>\Omega</math> to 43 <math>\Omega</math>.</p>
PDREQ SDREQ	<ul style="list-style-type: none"> <li>No extra series termination resistors.</li> <li>No pull-down resistors required.</li> </ul>	<ul style="list-style-type: none"> <li>These signals have integrated series resistors in the ICH3-S.</li> <li>These signals have integrated pull-down resistors in the ICH3-S.</li> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul>
PIORDY SIORDY	<ul style="list-style-type: none"> <li>No extra series termination resistors.</li> <li>Pull-up to VCC3.3 via a <math>4.7 \pm 5\%</math> k<math>\Omega</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>These signals have integrated series resistors in the ICH3-S.</li> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul>
IRQ14 IRQ15	<ul style="list-style-type: none"> <li>Recommend 8.2 k<math>\Omega</math> – 10 k<math>\Omega</math> pull-up resistors to VCC3.3.</li> <li>No extra series termination resistors.</li> </ul>	<ul style="list-style-type: none"> <li>Open drain outputs from drive.</li> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul>
IDERST#	<ul style="list-style-type: none"> <li>The PCIRST# signal should be buffered to form the IDERST# signal. A 33 <math>\Omega</math> series termination resistor is recommended on this signal.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul>

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 3 of 8)

Checklist Items	Recommendations	Comments
Cable Detect	<ul style="list-style-type: none"> <li>Host Side/Device Side Detection (recommended method):               <ul style="list-style-type: none"> <li>Connect IDE pin PDIAG#/CBLID# to an ICH3-S GPIO pin. Connect a 10 k<math>\Omega</math> resistor to GND on the signal line.</li> </ul> </li> <li>Device side detection:               <ul style="list-style-type: none"> <li>Connect a 0.047 <math>\mu</math>F capacitor from IDE pin PDIAG#/CBLID to GND. No ICH3-S connection.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>The 10 k<math>\Omega</math> resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs.</li> <li>Refer to <a href="#">Section 9.1.2.1</a>.</li> </ul> <p><b>NOTE:</b> All ATA66/ATA100 drives will have the capability to detect cables.</p>
<b>Interrupt Interface</b>		
APICCLK	<ul style="list-style-type: none"> <li>Pull-down directly to GND.</li> </ul>	
APICD[1:0]	<ul style="list-style-type: none"> <li>Use 10 k<math>\Omega \pm 5\%</math> pull-down resistor to Ground.</li> </ul>	
PIRQ[D:A]#	<ul style="list-style-type: none"> <li>These signals require a pull-up resistor.</li> <li>Recommend a 2.7 k<math>\Omega \pm 5\%</math> pull-up resistor to VCC_5 or an 8.2 k<math>\Omega \pm 5\%</math> pull-up resistor to VCC_3.3.</li> </ul>	<ul style="list-style-type: none"> <li>Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion:               <ul style="list-style-type: none"> <li>PIRQ[A]# is connected to IRQ16.</li> <li>PIRQ[B]# is connected to IRQ17.</li> <li>PIRQ[C]# is connected to IRQ18.</li> <li>PIRQ[D]# is connected to IRQ19.</li> </ul> </li> </ul> <p>This frees the ISA interrupts.</p>
PIRQ[H:E]#/ GPIO[5:2]	<ul style="list-style-type: none"> <li>These signals require a pull-up resistor.</li> <li>Recommend a 2.7 k<math>\Omega \pm 5\%</math> pull-up resistor to VCC5 or an 8.2 k<math>\Omega \pm 5\%</math> pull-up resistor to VCC3_3.</li> </ul>	<ul style="list-style-type: none"> <li>These signals are connected to the internal I/O APIC in the following fashion:               <ul style="list-style-type: none"> <li>PIRQ[E]# is connected to IRQ20.</li> <li>PIRQ[F]# is connected to IRQ21.</li> <li>PIRQ[G]# is connected to IRQ22.</li> <li>PIRQ[H]# is connected to IRQ23.</li> </ul> </li> </ul> <p>This frees the ISA interrupts.</p>
SERIRQ	<ul style="list-style-type: none"> <li>External weak (8.2 k<math>\Omega \pm 5\%</math>) pull-up resistor to VCC3_3 is recommended.</li> </ul>	<ul style="list-style-type: none"> <li>Open drain signal.</li> </ul>

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 4 of 8)

Checklist Items	Recommendations	Comments
<b>LAN Interface</b>		
LAN_CLK	<ul style="list-style-type: none"> <li>Connect to LAN_CLK on Platform LAN Connect Device.<sup>2</sup></li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 9.7</a>.</li> </ul>
LAN_RXD[2:0]	<ul style="list-style-type: none"> <li>Connect to LAN_RXD on Platform LAN Connect Device.<sup>2</sup></li> </ul>	<ul style="list-style-type: none"> <li>ICH3-S contains integrated 9 k<math>\Omega</math> pull-up resistors on interface.</li> <li>Refer to <a href="#">Section 9.7</a>.</li> </ul>
LAN_TXD[2:0], LAN_RSTSYNC	<ul style="list-style-type: none"> <li>Connect to LAN_TXD on Platform LAN Connect Device.<sup>2</sup></li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 9.7</a>.</li> </ul>
<b>Miscellaneous Signals</b>		
SPKR	<ul style="list-style-type: none"> <li>Has integrated pull-down.</li> </ul>	<ul style="list-style-type: none"> <li>The integrated pull-down is enabled only at boot/ reset for strapping functions. At all other times, the pull-down is disabled.</li> <li>Refer to <a href="#">Section 9.2</a>.</li> </ul>
TP[0]	<ul style="list-style-type: none"> <li>TP[0] requires external pull-up resistor to VCCSUS_3.3.</li> </ul>	
AC_SDOOUT	<ul style="list-style-type: none"> <li>Requires a jumper to 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCCSUS_3.3. Should not be stuffed for default operation.</li> </ul>	<ul style="list-style-type: none"> <li>This ball has a weak internal pull-down. To properly detect a safe_mode condition, a strong pull-up is required to override this internal pull down.</li> </ul>
EE_DOUT	<ul style="list-style-type: none"> <li>Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM.</li> </ul>	<ul style="list-style-type: none"> <li>ICH3-S contains an integrated pull-up resistor for this signal.</li> <li>Connect to EEPROM data input signal.</li> <li>(Input from EEPROM perspective and output from ICH3-S perspective.)</li> </ul>
EE_DIN	<ul style="list-style-type: none"> <li>No extra circuitry required. Connect to EE_DOUT of EEPROM.</li> </ul>	<ul style="list-style-type: none"> <li>ICH3-S contains an integrated pull-up resistor for this signal.</li> <li>Connect to EEPROM data input signal.</li> <li>(Output from EEPROM perspective and input from ICH3-S perspective.)</li> </ul>
<b>PCI Interface</b>		
PERR# SERR# PLOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ#[4:0] GPIO[0]/REQ[A]# GPIO[1]/REQ[B]#/ REQ[5]#	<ul style="list-style-type: none"> <li>These signals require a pull-up resistor. Recommend an 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCC3.3, or a 2.7 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCC5.</li> </ul>	<ul style="list-style-type: none"> <li>See the <i>PCI Local Bus Specification, Revision 2.2</i> for pull-up recommendations for VCC3_3 and VCC5.</li> </ul>
PCIRST#	<ul style="list-style-type: none"> <li>Depending on the load this signal may have to be buffered.</li> </ul>	<ul style="list-style-type: none"> <li>Improves Signal Integrity.</li> </ul>

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 5 of 8)

Checklist Items	Recommendations	Comments
GNT[4:0]#	<ul style="list-style-type: none"> <li>No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to VCC3.3.</li> </ul>	<ul style="list-style-type: none"> <li>These signals are actively driven by the ICH3-S.</li> </ul>
PME#	<ul style="list-style-type: none"> <li>No extra pull-up resistor.</li> </ul>	<ul style="list-style-type: none"> <li>This signal has integrated pull-up of 18 k<math>\Omega</math> to 42 k<math>\Omega</math>.</li> </ul>
GNT[A]# /GPIO[16] GNT[B]# / GNT[5]#/ GPIO[17]	<ul style="list-style-type: none"> <li>No extra pull-up needed.</li> </ul>	<ul style="list-style-type: none"> <li>These signals have integrated pull-ups of 24 k<math>\Omega</math>.</li> <li>GNT[A] has an added strap function of "top block swap." The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.</li> </ul>
<b>Power</b>		
V_CPU_IO[2:0]	<ul style="list-style-type: none"> <li>The power pins should be connected to the proper power plane for the processor CMOS compatibility signals. Use one 0.1 <math>\mu</math>F decoupling capacitor.</li> </ul>	<ul style="list-style-type: none"> <li>Used to pull-up all processor I/F signals.</li> </ul>
VCCRTC	<ul style="list-style-type: none"> <li>No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS.</li> </ul>	
VCC_3.3	<ul style="list-style-type: none"> <li>Use six 0.1 <math>\mu</math>F decoupling capacitors.</li> </ul>	
VCCSUS_3.3	<ul style="list-style-type: none"> <li>Use two 0.1 <math>\mu</math>F decoupling capacitors.</li> </ul>	
VCC_1.8	<ul style="list-style-type: none"> <li>Use four 0.1 <math>\mu</math>F decoupling capacitors.</li> </ul>	
VCCSUS_1.8	<ul style="list-style-type: none"> <li>Use one 0.1 <math>\mu</math>F decoupling capacitor.</li> </ul>	
V5_REF_SUS	<ul style="list-style-type: none"> <li>Use one 0.1 <math>\mu</math>F decoupling capacitor.</li> <li>V5REF_SUS is the reference voltage for some 5 V tolerant inputs in the ICH3-S. V5REF_SUS must power up before or simultaneous to VCCSUS3.3. It must power down after or simultaneous to VCCSUS3.3. (For most platforms this sequencing isn't an issues because VCCSUS3.3 is derived from V5SUS.</li> </ul>	
V5_REF	<ul style="list-style-type: none"> <li>Requires one 0.1 <math>\mu</math>F decoupling capacitor.</li> <li>V5_REF is the reference voltage for most 5V tolerant inputs in the ICH3-S. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC_3.3. It must power down after or simultaneous to VCC_3.3.</li> <li>If USB is implemented in the platform, V5REF_Sus must be connected to VSus5.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Figure 12-22</a> for an example circuit schematic that may be used to ensure the proper V5REF sequencing.</li> </ul>



Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 6 of 8)

Checklist Items	Recommendations	Comments
<b>Power Management</b>		
THRM#	<ul style="list-style-type: none"> <li>Connect to temperature Sensor. Pull-up if not used with an 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCC_3.3.</li> </ul>	<ul style="list-style-type: none"> <li>Input to ICH3-S cannot float. THRM# polarity bit defaults THRM# to active low, so pull up to VCC_3.3.</li> </ul>
SLP_S3# SLP_S5#	<ul style="list-style-type: none"> <li>No pull-up/down resistors needed. Signals driven by ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Signals driven by ICH3-S.</li> </ul>
PWR0K	<ul style="list-style-type: none"> <li>This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC_3.3 and VCC_1.8 have reached their nominal voltages.</li> <li>Use external weak pull-down (see <a href="#">Section 9.6.8</a>).</li> </ul>	<ul style="list-style-type: none"> <li>Timing Requirement.</li> </ul>
PWRBTN#	<ul style="list-style-type: none"> <li>No extra pull-up resistors.</li> </ul>	<ul style="list-style-type: none"> <li>This signal has an integrated pull-up of 18 k<math>\Omega</math> – 42 k<math>\Omega</math>.</li> </ul>
RI#	<ul style="list-style-type: none"> <li>RI# does not have an internal pull-up. Recommend an 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to resume well.</li> </ul>	<ul style="list-style-type: none"> <li>If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set, and the system will interpret that as a wake event.</li> </ul>
RSMRST#	<ul style="list-style-type: none"> <li>This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCCSUS3.3 and VCCSUS1.8 have reached their nominal voltages. Can be tied to LAN_RST# on server Platforms.</li> <li>Use external weak pull-down (see <a href="#">Section 9.6.8</a>).</li> </ul>	<ul style="list-style-type: none"> <li>Timing Requirement.</li> </ul>
SUS_STAT#	<ul style="list-style-type: none"> <li>Disconnect from ICH3-S and leave not connected. Use 8.2 k<math>\Omega</math> pull-up to VCC_3.3 for remaining devices on LPC bus.</li> </ul>	
DPRSLPVR	<ul style="list-style-type: none"> <li>Leave as no connect.</li> </ul>	<ul style="list-style-type: none"> <li>Integrated pull-down.</li> </ul>

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 7 of 8)

Checklist Items	Recommendations	Comments
<b>RTC</b>		
VBIAS	<ul style="list-style-type: none"> <li>The VBIAS pin of the ICH3-S is connected to a 0.047 <math>\mu</math>F capacitor.</li> </ul>	<ul style="list-style-type: none"> <li>For noise immunity on VBIAS signal.</li> <li>Refer to <a href="#">Figure 9-10</a>.</li> </ul>
RTCX1 RTCX2	<ul style="list-style-type: none"> <li>Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 M<math>\Omega</math> resistor. Decouple each signal using a 18 pF capacitor.</li> <li>RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3 V source.</li> </ul>	<ul style="list-style-type: none"> <li>The external circuitry shown in <a href="#">Figure 9-10</a> is required to maintain the accuracy of the RTC.</li> <li>Refer to <a href="#">Section 9.6.1</a></li> <li>The circuitry is required because the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on the power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.</li> <li>Refer to <a href="#">Section 9.6.2</a> for decoupling requirements.</li> </ul>
<b>System Management</b>		
SMBDATA SMBCLK	<ul style="list-style-type: none"> <li>Require external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors (core well, suspend well, or a combination).</li> <li>Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections.</li> <li>SMBCLK required to be tied to SMLink0 and SMBDATA required to be tied to SMLink1 for SMBus 2.0 compliance.</li> </ul>	<ul style="list-style-type: none"> <li>Value of pull-up resistors determined by line load. Typical value used is 8.2 k<math>\Omega</math> <math>\pm</math> 5%.</li> <li>Refer to <a href="#">Section 9.5</a>.</li> </ul>
SMBALERT#/ GPIO[11]	<ul style="list-style-type: none"> <li>See GPIO section if SMBALERT# not implemented.</li> </ul>	
SMLINK[1:0]	<ul style="list-style-type: none"> <li>Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)</li> <li>Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections.</li> <li>SMLink0 required to be tied to SMBCLK and SMLink1 required to be tied to SMBDATA for SMBus 2.0 compliance.</li> </ul>	<ul style="list-style-type: none"> <li>Value of pull-ups resistors determined by line load. Typical value used is 8.2 k<math>\Omega</math> <math>\pm</math> 5%.</li> <li>Refer to <a href="#">Section 9.5</a>.</li> </ul>
INTRUDER#	<ul style="list-style-type: none"> <li>Pull signal to VCCRTC (VBAT) if not needed.</li> </ul>	<ul style="list-style-type: none"> <li>Signal in VCCRTC (VBAT) well.</li> <li>Refer to <a href="#">Section 9.6.8</a>.</li> </ul>

**Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 8 of 8)**

Checklist Items	Recommendations	Comments
<b>USB</b>		
USBRBIAS	<ul style="list-style-type: none"> <li>Required <math>18.2\ \Omega \pm 1\%</math> pull-down.</li> </ul>	
USBP[5:0]P USBP[5:0]N	<ul style="list-style-type: none"> <li>No external resistors are required.</li> </ul>	<ul style="list-style-type: none"> <li>Integrated <math>15\ \text{k}\Omega</math> pull-down, effective output driver impedance of <math>45\ \Omega</math> provided.</li> </ul>
OC[5:0]#	<ul style="list-style-type: none"> <li>If not used, use <math>10\ \text{k}\Omega \pm 5\%</math> pull-up to VCCSUS3.3.</li> </ul>	<ul style="list-style-type: none"> <li>Inputs must not float.</li> </ul>

**NOTES:**

- LINT1 and LINT0 map to INTR and NMI in the ICH3-S.
- LAN Connect Interface Signals can be left as NC if not used because the Input buffers are internally terminated.

## 13.4 Intel® 82870P2 P64H2 Schematic Checklist

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
<b>Hub Interface</b>		
BPCLK100 BPCLK133	<ul style="list-style-type: none"> <li>These can be left as no connects.</li> </ul>	<ul style="list-style-type: none"> <li>These clock signals are used for testing modes.</li> </ul>
CLK200 CLK200#	<ul style="list-style-type: none"> <li>If not used, pull-up to VCC3.3 with an <math>8.2\text{ k}\Omega \pm 5\%</math> resistor.</li> </ul>	
HI_RCOMP	<ul style="list-style-type: none"> <li>For a <math>50\text{ }\Omega \pm 10\%</math> board, RCOMP = <math>61.9\text{ }\Omega \pm 1\%</math>. Connect to VCC1.8. The trace length between the P64H2 pin and the resistor lead should be <math>&lt; 1"</math>.</li> </ul>	
HI_VREF HI_VSWING	<ul style="list-style-type: none"> <li>P64H2 Hub reference swing voltage = <math>0.800\text{ V} \pm 5\%</math>.</li> <li><math>R4 = 261\text{ }\Omega \pm 1\%</math>, <math>R5 = 332\text{ }\Omega \pm 1\%</math>, <math>R6 = 750\text{ }\Omega \pm 1\%</math>.</li> <li><math>C1 = 0.1\text{ }\mu\text{F}</math>, <math>C2 = 0.01\text{ }\mu\text{F}</math>.</li> <li>Refer to <a href="#">Figure 7-5</a> and <a href="#">Figure 7-8</a>.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.2.2</a> and for circuit implementation.</li> </ul>
HI_[19]	<ul style="list-style-type: none"> <li>HI[19] can be left as no connect if parity is not going to be used.</li> </ul>	
<b>PCI/PCI-X Bus Interface</b>		
PxAD[63:32] PxC/BE#[7:4] PxDEVSEL# PxFRAME# PxIRDY# PxTRDY# PxSTOP# PxPERR# PxSERR# PxREQ[5:0]# PxPLOCK# PxPAR64 PxACK64# PxREQ64#	<ul style="list-style-type: none"> <li><math>8.2\text{ k}\Omega \pm 5\%</math> pull-up resistor to VCC3.3.</li> </ul>	<ul style="list-style-type: none"> <li>See PCI Specification Rev 2.2.</li> </ul>
PAGNT3#	<ul style="list-style-type: none"> <li>CLK66 Mode: <math>8.2\text{ k}\Omega \pm 5\%</math> pull-down to ground.</li> <li>CLK200 Mode: <math>8.2\text{ k}\Omega \pm 5\%</math> pull-up to VCC_3.3.</li> </ul>	<ul style="list-style-type: none"> <li>1 = Use CLK66. 0 = Use CLK200/CLK200#.</li> </ul>
PBGNT3#	<ul style="list-style-type: none"> <li>Connect to ground through an <math>8.2\text{ k}\Omega \pm 5\%</math> pull-down resistor.</li> </ul>	
GNT[A]#/ GPIO[16] GNT[B]/ GNT[5]#/ GPIO[17]	<ul style="list-style-type: none"> <li>No extra pull-up needed.</li> </ul>	<ul style="list-style-type: none"> <li>These signals have integrated pull-ups of <math>24\text{ k}\Omega</math>.</li> </ul>

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
PCIXCAP	<ul style="list-style-type: none"> <li>Conventional PCI cards connect this pin directly to ground.</li> <li>PCI-X 133 cards connect PCIXCAP to ground through a <math>0.01\ \mu\text{F} \pm 10\%</math> capacitor to provide an AC signal return path.</li> <li>PCI-X 66 cards connect PCIXCAP to ground through a <math>10\ \text{k}\Omega \pm 5\%</math> resistor in parallel with a <math>0.01\ \mu\text{F} \pm 10\%</math> capacitor to provide an AC signal return path.</li> <li>If implementing hot plug, PCIXCAP should be pulled up to VCC3.3 through an <math>8.2\ \text{k}\Omega \pm 5\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>See PCI-X Specification 1.0 recommendations for PCIXCAP connection.</li> </ul>
PA_133EN	<ul style="list-style-type: none"> <li>Enable PCI-X at 133 MHz for PCI Bus A. This pin, when high, allows the PCI-X segment to run at 133 MHz when PA_PCIXCAP is sampled high. When low, the PCI-X segment runs only at 100 MHz when PA_PCIXCAP is sampled high.</li> <li>For 133 MHz (max) PCI-X capable slot: <math>8.2\ \text{k}\Omega \pm 5\%</math> pull-up resistor to VCC3.3.</li> <li>For 100 MHz (max) PCI-X capable slot: <math>8.2\ \text{k}\Omega \pm 5\%</math> pull-down resistor to ground.</li> </ul>	<ul style="list-style-type: none"> <li>Active only if PA_PCIXCAP pin is high.</li> </ul>
PB_133EN	<ul style="list-style-type: none"> <li>Enable PCI-X at 133MHz for PCI Bus B. This pin, when high, allows the PCI-X segment to run at 133 MHz when PB_PCIXCAP is sampled high. When low, the PCI-X segment runs only at 100 MHz when PB_PCIXCAP is sampled high.</li> <li>For 133 MHz (max) PCI-X capable slot: <math>8.2\ \text{k}\Omega \pm 5\%</math> pull-up resistor to VCC3.3.</li> <li>For 100MHz (max) PCI-X capable slot: <math>8.2\ \text{k}\Omega \pm 5\%</math> pull-down resistor to ground.</li> </ul>	<ul style="list-style-type: none"> <li>Active only if PB_PCIXCAP pin is high.</li> </ul>
IDSEL	<ul style="list-style-type: none"> <li>The series resistor on IDSEL should be <math>100\ \Omega</math>.</li> </ul>	<ul style="list-style-type: none"> <li>This has changed from the PCI-X 1.0 Specification. There is a specification change that allows for values other than the original <math>2\ \text{k}\Omega</math> value.</li> </ul>
3.3Vaux	<ul style="list-style-type: none"> <li>Leave this as unconnected on the PCI slots.</li> </ul>	<ul style="list-style-type: none"> <li>The P64H2 does not support PCI bus power management.</li> </ul>
<b>PCI-X Specific Interface</b>		
PCIXCAP	<ul style="list-style-type: none"> <li>Conventional PCI cards connect this pin directly to ground.</li> <li>PCI-X 133 cards connect PCIXCAP to ground through a <math>0.01\ \mu\text{F} \pm 10\%</math> capacitor to provide an AC signal return path. PCI-X 66 cards connect PCIXCAP to ground through a <math>10\ \text{k}\Omega \pm 5\%</math> resistor in parallel with a <math>0.01\ \mu\text{F} \pm 10\%</math> capacitor to provide an AC signal return path.</li> <li>If implementing hot plug, PCIXCAP should be pulled up to VCC_3.3 through an <math>8.2\ \text{k}\Omega</math> resistor. If not implementing hot plug, this signal does not require a pull up or pull down.</li> </ul>	<ul style="list-style-type: none"> <li>See <i>PCI-X Specification</i> recommendations for PCIXCAP connection.</li> </ul>

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
PA_133EN PB_133EN	<ul style="list-style-type: none"> <li>Enable PCI-X at 133 MHz for PCI Bus A. This pin, when high, allows the PCI-X segment to run at 133 MHz when PA_PCIXCAP is sampled high. When low, the PCI-X segment will run only at 100 MHz when PA-PCIXCAP is sampled high. <ul style="list-style-type: none"> <li>For 133 MHz (max) PCI-X capable slot: 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCC_3.3.</li> <li>For 100 MHz (max) PCI-X capable slot: 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-down resistor to ground.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>Only active if PA_PCIXCAP and PB_PCIXCAP pins are high, respectively.</li> </ul>
<b>Interrupt Interface</b>		
PAIRQ[15:0] PBIRQ[15:0]	<ul style="list-style-type: none"> <li>Unused PxlRQ lines should be terminated using an 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCC3.3.</li> </ul>	
APICCLK APICD[1:0]	<ul style="list-style-type: none"> <li>If APIC is not used, terminate using an 8.2 k<math>\Omega</math> <math>\pm</math> 5% pull-up resistor to VCC3.3.</li> </ul>	
<b>Hot Plug Interface</b>		
PCIXCAP (On P64H2 Hot Plug Interface)	<ul style="list-style-type: none"> <li>If implementing hot plug, PCIXCAP should be pulled up to VCC3.3 through an 8.2 k<math>\Omega</math> <math>\pm</math> 5% resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Unused inputs should not float.</li> </ul>
M66EN (On P64H2 Hot Plug Interface)	<ul style="list-style-type: none"> <li>If implementing hot plug, M66EN should be pulled up to VCC3.3 through a 5 k<math>\Omega</math> <math>\pm</math> 5% resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Unused inputs should not float.</li> </ul>
SWITCH	<ul style="list-style-type: none"> <li>Connect to MRL Sensor. Open MRL should pull HxSWITCH to VCC3.3. Closed MRL should pull HxSWITCH to GND.</li> </ul>	
PRSNT1# PRSNT2#	<ul style="list-style-type: none"> <li>Pull-up to VCC3.3 through a 5.6 k<math>\Omega</math> <math>\pm</math> 5% resistor.</li> <li>If implementing Attention Button, PRSNT1# is the XOR of the momentary push-button and Slot Present signal.</li> </ul>	
PxAD[63:32] PxC/BE[7:4] PxPAR PxPAR64 PxREQ64# PxACK64# PxFRAME# PxIRDY# PxTRDY# PxSTOP# PxDEVSEL# PxPLOCK# PxPERR# PxSERR# PxREQ[5:0]#	<ul style="list-style-type: none"> <li>If implementing hot plug, pull up to VCC3.3 through an 8.2 k<math>\Omega</math> <math>\pm</math> 5% resistor.</li> </ul>	<ul style="list-style-type: none"> <li>See PCI 2.2 specification.</li> </ul>

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
<b>Hot Plug – Single Slot Parallel Mode Specific</b>		
PxIRQ[14:8] <sup>1</sup>	<ul style="list-style-type: none"> <li>Pulled to 3.3 Vcc through an 8.2 kΩ ± 5% resistor.</li> </ul>	<ul style="list-style-type: none"> <li>These signals are mapped to hot plug functions in single slot hot plug mode.</li> </ul>
HPx_SLOT[2:0] <sup>1</sup>	SLOT[0]: Use an 8.2 kΩ pull-up to VCC_3.3. SLOT[1]: Use an 8.2 kΩ pull-down to ground. SLOT[2]: Use an 8.2 kΩ pull-down to ground.	<ul style="list-style-type: none"> <li>This is a strapping pin for enabling Single Slot Parallel Mode which is latched during reset. SLOT[1] also functions as the HxPCIXCAP2A input when not in reset. SLOT2 also functions as the HxPCIXCAP1A input when not in reset. Refer to <a href="#">Table 8-8</a>.</li> </ul>
PxIRQ[15] <sup>1</sup>	<ul style="list-style-type: none"> <li>Pulled to 3.3 Vcc through an 8.2Ω – 10 kΩ resistor.</li> </ul>	<ul style="list-style-type: none"> <li>A logic 1 on this pin indicates to the controller that the PCI slot should be immediately powered off. This signal is also connected to a SPST switch to ground which, when pressed, indicates by means of a logic 0 that the slot can be powered on.</li> </ul>
<b>Hot Plug – Dual Slot Parallel Mode Specific</b>		
HPx_SLOT[2:0] <sup>1</sup>	SLOT[0]: Use an 8.2 kΩ pull-down to ground. SLOT[1]: Use an 8.2 kΩ pull-up to VCC_3.3. SLOT[2]: Use an 8.2 kΩ pull-down to ground.	<ul style="list-style-type: none"> <li>This is a strapping pin for enabling Single Slot Parallel Mode which is latched during reset. SLOT[1] also functions as the HxPCIXCAP2A input when not in reset. SLOT2 also functions as the HxPCIXCAP1A input when not in reset. Refer to <a href="#">Table 8-8</a>.</li> </ul>
PxIRQ[15] <sup>1</sup> PxIRQ[10] <sup>1</sup>	<ul style="list-style-type: none"> <li>Pulled to 3.3 Vcc through an 8.2 – 10 kΩ ± 5% resistor.</li> </ul>	<ul style="list-style-type: none"> <li>A logic 1 on this pin indicates to the controller that the PCI slot should be immediately powered off. This signal is also connected to a SPST switch to ground which when pressed indicates by means of a logic 0 that the slot can be powered on.</li> </ul>
PxIRQ[9:8] <sup>1</sup> PxIRQ[14:11] <sup>1</sup>	<ul style="list-style-type: none"> <li>Pulled to 3.3 Vcc through an 8.2 kΩ ± 5% resistor.</li> </ul>	<ul style="list-style-type: none"> <li>These signals are mapped to hot plug functions in dual slot hot plug mode.</li> </ul>
PPxSID <sup>1</sup>	<ul style="list-style-type: none"> <li>In dual-slot Hot Plug mode, connect this signal to ground through an 8.2 kΩ ± 5% pull-down resistor.</li> </ul>	<ul style="list-style-type: none"> <li>This insures that the LED for slot B on busses A and B remain off during reset.</li> </ul>
<b>Hot Plug – Serial Mode Specific</b>		
HPx_SLOT[2:0] <sup>1</sup>	<ul style="list-style-type: none"> <li>Pulled to VCC_3.3 or ground through an 8.2 kΩ ± 5% resistor depending on the number of PCI hot plug slots to be enabled.</li> </ul>	<ul style="list-style-type: none"> <li>This is a strapping pin for enabling Serial Mode.</li> </ul>

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
<b>Hot Plug – Disabled</b>		
HPxSLOT[2:0]	<ul style="list-style-type: none"> <li>If disabling hot plug mode, connect these signals to ground through an <math>8.2\text{ k}\Omega \pm 5\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>HPxSLOT[2:0] signals should be strapped to zero to disable hot plug mode.</li> </ul>
HPx_SID	<ul style="list-style-type: none"> <li>Connect to ground through an <math>8.2\text{ k}\Omega \pm 5\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Unused inputs should not float.</li> </ul>
HPx_SIC HPx_SIL# HPx_SOR# HPx_SORR# HPx_SOC HPx_SOL HPx_SOLR HPx_SOD	<ul style="list-style-type: none"> <li>If disabling hot plug mode, these signals can be left as no connect.</li> </ul>	
PCIXCAP	<ul style="list-style-type: none"> <li>This signal does not need a pull-up or a pull-down resistor when hot plug is disabled.</li> </ul>	
<b>SMBus Interface</b>		
SDTA SCLK	<ul style="list-style-type: none"> <li>Use an <math>8.2\text{ k}\Omega \pm 5\%</math> pull-up resistor to VCC_3.3.</li> </ul>	
<b>Power</b>		
VCC	<ul style="list-style-type: none"> <li>Connect to 1.8 V power supply.</li> <li>Decoupling: <ul style="list-style-type: none"> <li>– 8 X <math>0.1\text{ }\mu\text{F}</math> capacitors near the P64H2.</li> <li>– 2 X <math>4.0\text{ }\mu\text{F}</math> capacitors near regulator.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>1.8 V Core Voltage.</li> </ul>
VCC1.8	<ul style="list-style-type: none"> <li>Connect to 1.8 V Power Supply.</li> <li>Decoupling: <ul style="list-style-type: none"> <li>– 2 X <math>1.0\text{ }\mu\text{F}</math> capacitors near the P64H2.</li> <li>– 1 X <math>100.0\text{ }\mu\text{F}</math> capacitors near regulator.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>1.8 V Hub Interface Voltage.</li> </ul>
VCC3.3	<ul style="list-style-type: none"> <li>Connect to 3.3 V Power Supply.</li> <li>Decoupling: <ul style="list-style-type: none"> <li>– 20 <math>0.1\text{ }\mu\text{F}</math> capacitors near the P64H2.</li> <li>– 6 X <math>1.0\text{ }\mu\text{F}</math> capacitors near the P64H2.</li> <li>– 2 X <math>4.0\text{ }\mu\text{F}</math> capacitors near regulator.</li> <li>– 1 X <math>100.0\text{ }\mu\text{F}</math> capacitors near regulator.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>3.3 V.</li> </ul>
VCC5REF	<ul style="list-style-type: none"> <li>Connect to 5 V Power Supply.</li> </ul>	<ul style="list-style-type: none"> <li>5 V.</li> </ul>
<b>Miscellaneous Signals</b>		
TP0	<ul style="list-style-type: none"> <li><math>8.2\text{ k}\Omega \pm 5\%</math> pull-up resistor to VCC3.3.</li> </ul>	
RSTIN#	<ul style="list-style-type: none"> <li>Connect to the PCIRST# output of the ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Reset In. When asserted, this signal asynchronously resets the P64H2 logic and asserts PCIRST# active output from each PCI interface.</li> </ul>
TEST#	<ul style="list-style-type: none"> <li><math>8.2\text{ k}\Omega \pm 5\%</math> pull-up resistor to VCC3.3.</li> </ul>	<ul style="list-style-type: none"> <li>Intel Test Mode.</li> </ul>
RASERR#	<ul style="list-style-type: none"> <li><math>8.2\text{ k}\Omega \pm 5\%</math> pull-up resistor to VCC3.3.</li> </ul>	

**NOTE:**

1. x = A or B



## 13.5 CK408 Schematic Checklist

Table 13-5. CK408 Schematic Checklist

Checklist Items	Recommendations	Reason/Impact
66BUFF[2:0]	<ul style="list-style-type: none"> <li>Connect to a P64H2 using a series <math>43\ \Omega \pm 5\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.2</a>.</li> </ul>
66IN	<ul style="list-style-type: none"> <li>No Connect.</li> </ul>	
3V66_0	<ul style="list-style-type: none"> <li>Connect to ICH3-S using a series <math>43\ \Omega \pm 5\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.2</a>.</li> </ul>
3V66_1_VCH	<ul style="list-style-type: none"> <li>Connect to MCH using a series <math>43\ \Omega \pm 5\%</math> resistor.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.2</a>.</li> </ul>
CPU[3:0] CPU[3:0]#	<ul style="list-style-type: none"> <li>Connect to the processor, MCH, or ITP using a series <math>33\ \Omega \pm 5\%</math> resistor, and terminate to GND through a <math>49.9\ \Omega \pm 1\%</math> resistor. On the ITP port, use a <math>10\ \text{k}\Omega \pm 5\%</math> pull-up resistor to V3_CLK close to CK408B.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.1</a>.</li> </ul>
DOT_48MHz	<ul style="list-style-type: none"> <li>No Connect.</li> </ul>	
IREF	<ul style="list-style-type: none"> <li>Terminate to GND through a <math>475\ \Omega \pm 1\%</math> resistor.</li> </ul>	
MULT0	<ul style="list-style-type: none"> <li>Terminate to V3_CLK through a series <math>10\ \text{k}\Omega \pm 5\%</math> resistor.</li> </ul>	
PCI[4:0]	<ul style="list-style-type: none"> <li>Connect to a series <math>33\ \Omega \pm 5\%</math> resistor for PCI33_CLK33, VIDEO_CLK33, FWH_CLK33, SIO_CLK33, and LPC_CLK33.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.4</a>.</li> </ul>
PCI[6:5]	<ul style="list-style-type: none"> <li>No Connect.</li> </ul>	
PCIF[0]	<ul style="list-style-type: none"> <li>Connect to a series <math>33\ \Omega \pm 5\%</math> resistor for ICH3_CLK33.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.3</a>.</li> </ul>
PCIF[2:1]	<ul style="list-style-type: none"> <li>No Connect.</li> </ul>	
PCI_STOP#	<ul style="list-style-type: none"> <li>Terminate to V3_CLK through a <math>10\ \text{k}\Omega \pm 5\%</math> resistor.</li> </ul>	
PWRDWN#	<ul style="list-style-type: none"> <li>Connect to SLP_S3_N.</li> </ul>	
REF0	<ul style="list-style-type: none"> <li>Connect to a series <math>22\ \Omega \pm 5\%</math> resistor for CLK 14 output to LPC, VIDEO, SIO and ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.5</a>.</li> </ul>
SEL[1]	<ul style="list-style-type: none"> <li>Terminate to V3_CLK through a <math>10\ \text{k}\Omega \pm 5\%</math> resistor, and terminate to GND through a <math>10\ \text{k}\Omega \pm 5\%</math> resistor.</li> </ul>	
SCLK, SDTA	<ul style="list-style-type: none"> <li>Connect to 3V SMBus partition.</li> </ul>	
USB_48MHz	<ul style="list-style-type: none"> <li>Connect to ICH3-S using a <math>33\ \Omega \pm 5\%</math> series resistor to ICH3_CLK48.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.6</a>.</li> </ul>
VDD, VDD_48MHz VDDA	<ul style="list-style-type: none"> <li>Terminate to V3_CLK_A.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.3</a>.</li> </ul>
VSS, VSS_48MHz VSS_IREF	<ul style="list-style-type: none"> <li>Terminate to GND.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.3</a>.</li> </ul>
VTT_PWRGD#	<ul style="list-style-type: none"> <li>Terminate to GND through <math>1\ \text{k}\Omega \pm 5\%</math> resistor.</li> </ul>	
XTAL_IN XTAL_OUT	<ul style="list-style-type: none"> <li>Terminate to GND.</li> </ul>	

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# Layout Checklist

# 14

## 14.1 Processor Checklist

Table 14-1. Processor Layout Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments
A20M# IGNNE# INIT# LINT0/INTR LINT1/NMI PWRGOOD SMI# SLP# STPCLK#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S.</li> <li>Trace impedance = <math>50 \Omega \pm 10\%</math>.</li> <li>Route traces using 5/10 mil spacing.</li> <li>Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ SS I/O.</li> <li>Maximum agent to agent length is 9". Place pull-up resistor within 3" of Processor 1.</li> </ul>	<ul style="list-style-type: none"> <li>Asynchronous GTL+ Input Signals.</li> <li>Refer to <a href="#">Section 5.3.2</a>.</li> </ul>
A[35:3]# <sup>1</sup> ADSTB[1:0]# <sup>2</sup> DSTBN[3:0]# <sup>3</sup> DSTBP[3:0]# <sup>4</sup> DBI[3:0]# D[63:0]# <sup>5</sup> REQ[4:0]# <sup>6</sup>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Table 5-2</a>. Balance signal lengths within each strobe group.</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Source Synchronous I/O.</li> <li>Refer to <a href="#">Section 5.1</a>.</li> </ul>
ADS# AP[1:0] BINIT# BNR# BPM[5:0]# BRO# DBSY# DP[3:0]# DRDY# HIT# HITM# LOCK# MCERR# BPRI# BR[3:0]# DEFER# RESET# <sup>7</sup> RS[2:0]# RSP# TRDY# <sup>8</sup>	<ul style="list-style-type: none"> <li>Trace impedance = <math>50 \Omega \pm 10\%</math>.</li> <li>Route traces using 5/15 mil spacing.</li> <li>Do not route a stub to Processor 1.</li> <li>Keep signals on the same layer for the entire length of the bus.</li> <li>Route traces with at least 50% of the trace width directly over a reference plane.</li> <li>The distance from the pin of one agent to the pin of the next must be between 3" and 10".</li> <li>Total bus length must not exceed 20".</li> </ul>	<ul style="list-style-type: none"> <li>AGTL+ Common Clock Signals.</li> <li>Asserted to indicate the validity of the transaction address on the A[35:3]#<sup>1</sup> pins.</li> <li>Refer to <a href="#">Section 5.2</a>.</li> </ul>
BCLK[1:0]	<ul style="list-style-type: none"> <li>BCLKs to all processors should be length matched, and the BCLK to the MCH should be offset accordingly. See <a href="#">Table 4-3</a>.</li> </ul>	<ul style="list-style-type: none"> <li>System Bus Clock.</li> <li>Refer to <a href="#">Section 4.1.1</a>.</li> </ul>
FERR# IERR# PROCHOT# THERMTRIP#	<ul style="list-style-type: none"> <li>Connect to both processors and ICH3-S.</li> <li>Trace impedance = <math>50 \Omega \pm 10\%</math>.</li> <li>Route traces using 5/15 mil spacing.</li> <li>Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ SS I/O.</li> <li>Maximum agent to agent length is 10". Place pull-up resistor within 3" of Processor 1 and ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Async GLT+ Output.</li> <li>Refer to <a href="#">Section 5.3.1</a>.</li> </ul>

Table 14-1. Processor Layout Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments
COMP[1:0] ODTEN SKTOCC# TESTHI[6:0] VID[4:0]	<ul style="list-style-type: none"> <li>There are no routing requirements for these signals.</li> </ul>	<ul style="list-style-type: none"> <li>Enables processor on-die termination.</li> <li>Input.</li> <li>Refer to <a href="#">Section 5.3</a>.</li> </ul>
Reserved	<ul style="list-style-type: none"> <li>Reserved signals must remain as a No Connect (NC).</li> </ul>	
SM_ALERT# SM_CLK SM_DAT SM_EP_A[2:0] SM_TS_A[1:0] SM_WP	<ul style="list-style-type: none"> <li>Should be connected to the SMBus controller on 3.3 V partition.</li> </ul>	<ul style="list-style-type: none"> <li>SMBus I/O.</li> <li>Refer to <a href="#">Section 5.3.4</a>.</li> </ul>
VCCA	<ul style="list-style-type: none"> <li>To satisfy damping requirements, total series resistance in the filter (from VCC_CPU to the top plate of the capacitor) must be at least 0.35 <math>\Omega</math>. It includes the minimum DCR of the inductor, and any resistance (routing or discrete components) between VCC_CPU and capacitor top plate.</li> <li>The total maximum resistance cannot be greater than 1.1 <math>\Omega</math> as measured from VCC (more specifically, the baseboard via that connects the PLL filter to the VCC plane) to the processor VCCA interposer pin. Also, maximum trace resistance from the filter capacitor to processor socket pin should be less than 0.02 <math>\Omega</math>.</li> </ul>	<ul style="list-style-type: none"> <li>An isolated power for internal PLL.</li> <li>Refer to <a href="#">Section 12.2.8</a>.</li> </ul>
VSSA VCCIOPLL	<ul style="list-style-type: none"> <li>There are no routing requirements for these signals.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 12.2.8</a>.</li> </ul>
VCCSENSE VSSSENSE	<ul style="list-style-type: none"> <li>Route traces using 5/15 mil spacing.</li> <li>Place via next to the processor socket's pin for measurement of VCC_CPU/VSS.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 12.2.3</a>.</li> </ul>

**NOTES:**

1. A[35:3]# pins on the processor correspond to HA[35:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. DSTBN[3:0]# pins on the processor correspond to HADSTBN[3:0]# pins on the MCH.
4. DSTBP[3:0]# pins on the processor correspond to HADSTBP[3:0]# pins on the MCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.

## 14.2 Intel® E7500 MCH Layout Checklist

Table 14-2. MCH Layout Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments
<b>Host Interface</b>		
ADS# AP[1:0] BINIT# BNR# BPRI# BREQ0# <sup>1</sup> CPURST# <sup>2</sup> DBSY# DEFER# HA[35:3]# <sup>3</sup> HD[63:0]# <sup>4</sup> HADSTB[1:0]# <sup>5</sup> HDSTBN[3:0]# <sup>6</sup> HDSTBP[3:0]# <sup>7</sup> HIT# HITM# HLOCK# HREQ[4:0]# <sup>8</sup> HTRDY# <sup>9</sup> DP[3:0]# DRDY# RS[2:0]# RSP# XERR# <sup>10</sup> DBI[3:0]#	<ul style="list-style-type: none"> <li>See processor section of this checklist.</li> </ul>	
<b>DDR Interfaces A &amp; B / Connector</b>		
General Guidelines	<ul style="list-style-type: none"> <li>Route interface 50 <math>\Omega</math> nominal impedance, <math>\pm 10\%</math>.</li> <li>5 on 15 is maintained for Data/Strobe/CMD signals; 5 on 7 is maintained for CK/CK# signals.</li> <li>If using the recommended stackup, outer layer routing of DDR signals should be kept to a minimum (except for reference voltages). Via up close to passive devices, and immediately via back down following the device.</li> <li>Try to maintain same ground reference when transitioning layers—add stitching via if reference plane changes.</li> <li>Connect termination resistors directly to termination plane (flood is on outer layer).</li> <li>Space traces out as much as possible through the DIMMs.</li> <li>All traces are routed 1.8" to 6.0" from MCH to first DIMM connector, and 0.8" to 1.2" between connectors.</li> </ul>	

Table 14-2. MCH Layout Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments
DQ[63:0] CB[7:0] DQS[17:0]	<ul style="list-style-type: none"> <li>Route entirely on the same layer from MCH to DIMM to termination (no layer transitions). Place the 10 <math>\Omega</math> series resistor &lt; 800 mils from the first DIMM connector. All signals in a data group must be length matched to the associated DQS within <math>\pm 100</math> mils. In addition, each DQS must be length matched to its associated command clock within <math>\pm 1.75</math>". Place termination resistor within 800 mils from the last DIMM connector.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.2</a>.</li> </ul>
RAS# CAS# WE# MA[12:0] BA[1:0]	<ul style="list-style-type: none"> <li>Length match to command clock within 2 in. Place termination resistor within 800 mils from last DIMM connector. No more than 2 vias/layer transitions, not including breakout and passive devices.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.4</a>.</li> </ul>
CS[7:0]#	<ul style="list-style-type: none"> <li>Place termination resistor within 3" from the connector.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.5</a>.</li> </ul>
CMDCLK[3:0] CMDCLK[3:0]#	<ul style="list-style-type: none"> <li>Clock signals within a differential pair must be matched to each other within <math>\pm 2</math> mils. These signals must be routed 5 on 15, and must be at least 20 mils away from any other signal. Total length must be between 2.1" and 10.0".</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.3</a>.</li> </ul>
CKE	<ul style="list-style-type: none"> <li>Route 40 <math>\Omega</math> using a 7.5 mil wide trace. The CKE signal must be length matched to the clock signal at each DIMM within 2". Place termination resistor within 800 mils from last DIMM connector.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.5</a>.</li> </ul>
RCVENIN# RCVENOUT#	<ul style="list-style-type: none"> <li>RCVEN signal must be 15" <math>\pm 100</math> mils long, pulled up to VTT using 47 <math>\Omega \pm 2\%</math>.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.7</a>.</li> </ul>
DDRCOMP	<ul style="list-style-type: none"> <li>Place pull-up resistor within 1" of the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.8</a>.</li> </ul>
DDRCVOL DDRCVOH	<ul style="list-style-type: none"> <li>Place resistive network within 1" of the MCH.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.8</a>.</li> </ul>
Decoupling	<ul style="list-style-type: none"> <li>Spread termination decoupling capacitors evenly around the termination plane.</li> <li>Spread 2.5 V decoupling capacitors evenly around the DIMMs.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.11</a>.</li> </ul>
<b>Hub Interfaces</b>		
General Guidelines	<ul style="list-style-type: none"> <li>Hublink data spacing of 5 on 15 is maintained for data, and 5 on 35 is maintained for strobes.</li> <li>Traces are spaced out as much as possible through the BGA.</li> <li>Hublink data group signals are routed on the same layer, transitioning together if a layer change is required.</li> <li>Maximum length of 20" (stripline routing).</li> <li>Length match HI 2.0 strobes within 1" from data. Length match according to <a href="#">Figure 7-2</a>.</li> <li>HI 1.5: Length match strobes and data <math>\pm 100</math> mils.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.2.1</a> and <a href="#">Section 7.3.1</a> of this document.</li> </ul>

Table 14-2. MCH Layout Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments
<b>Clocks, Reset, Miscellaneous Signals</b>		
HCLKINP HLCKINN	<ul style="list-style-type: none"> <li>HCLKs should be length matched to all processors BCLKs. See <a href="#">Table 4-3</a> for routing guidelines.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.1</a>.</li> </ul>
CLK66	<ul style="list-style-type: none"> <li>Place series resistor close to CK408B.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 4.1.2</a>.</li> </ul>
RSTIN#	<ul style="list-style-type: none"> <li>Connect to PCIRST# output of the ICH3-S.</li> </ul>	
<b>Miscellaneous Signals</b>		
XORMODE#		
HIRCOMP_x HIVREF[D:A] HISWNG_[D:A]	<ul style="list-style-type: none"> <li>RCOMP, VOH, VOL, VSWING, VREF resistor networks are no more than 1" away from the MCH, and trace width is greater than 15 mils.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.2.2</a>, <a href="#">Section 7.2.3</a>, <a href="#">Section 7.3.2</a>, and <a href="#">Section 7.3.3</a>.</li> </ul>
HXRCOMP HYRCOMP		<ul style="list-style-type: none"> <li>This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic.</li> <li>Refer to <a href="#">Section 5.3.5</a>.</li> </ul>
<b>Voltage References – Power Planes</b>		
HVDREF[3:0] HAVREF[1:0] HCCVREF	<ul style="list-style-type: none"> <li>Use one dedicated voltage divider for all these signals. Decouple the voltage divider with a 1 <math>\mu</math>F capacitor.</li> </ul>	<ul style="list-style-type: none"> <li>To provide constant and clean power delivery to the data, address, and common clock signals of the host AGTL+ interface.</li> <li>Refer to <a href="#">Section 12.2.10</a>.</li> </ul>
VREF_DDR[5:0]		<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 6.8</a>.</li> </ul>
HXSWING HYSWING		<ul style="list-style-type: none"> <li>The HXSWING and HYSWING inputs of MCH are used to provide reference voltage for the compensation logic.</li> <li>Refer to <a href="#">Section 5.3.5</a>.</li> </ul>
VCCA	<ul style="list-style-type: none"> <li>High frequency decoupling for VCCA planes is located as close as possible to the associated MCH ball.</li> </ul>	

**NOTES:**

1. The BREQ0# pin on the MCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the MCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the MCH correspond to A[35:3]# pins on the processor.
4. HD[63:0]# pins on the MCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the MCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the MCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the MCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the MCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the MCH corresponds to the TRDY# pin on the processor.
10. The MCH XERR# pin can be connected to the processor IERR# pin or the processor MCERR# pin.

## 14.3 Intel® ICH3-S Layout Checklist

Table 14-3. Intel® ICH3-S Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
<b>Processor Signals</b>		
A20M# CPUSLP# FERR# IGNNE# INIT# LINT[1:0] SMI# STPCLK#	<ul style="list-style-type: none"> <li>See processor section of this checklist.</li> </ul>	
<b>FWH Interface</b>		
Decoupling	<ul style="list-style-type: none"> <li>0.1 <math>\mu</math>F capacitors should be placed between the VCC supply balls and the VSS ground balls, and no less than 390 mils from the VCC supply balls.</li> <li>4.7 <math>\mu</math>F capacitors should be placed between the VCC supply balls and the VSS ground balls, and no less than 390 mils from the VCC supply balls.</li> </ul>	
<b>Hub Interface</b>		
General Guidelines	<ul style="list-style-type: none"> <li>Board impedance must be 50 <math>\Omega \pm 10\%</math>.</li> <li>Traces must be routed 5 mils wide with 20 mils spacing (using given example 4-layer 4.5 mil prepreg stackup).</li> <li>To breakout of the MCH and ICH3-S package, the hub interface signals can be routed 5 on 5. Signals must be separated to 5 on 20 within 300 mils of the package.</li> <li>Maximum length of 20" (stripline routing).</li> <li>Data signals must be matched within <math>\pm 0.1</math>" of the HI_STB differential pair.</li> <li>HIREF dividers should be placed no more than 3.5 inches from MCH or ICH3-S.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 7.3</a>.</li> </ul>
<b>IDE Checklist</b>		
General Guidelines	<ul style="list-style-type: none"> <li>Traces are routed 5 mil wide with 7 mil spacing.</li> <li>Max trace length is 8" long.</li> <li>The maximum length difference between the longest and shortest trace length is 0.5".</li> </ul>	<ul style="list-style-type: none"> <li>Refer to ATA ATAPI-4 specification.</li> <li>Refer to <a href="#">Section 9.1.3</a> and <a href="#">Section 9.1.4</a>.</li> </ul>



Table 14-3. Intel® ICH3-S Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
<b>LAN Interface</b>		
General Guidelines	<ul style="list-style-type: none"> <li>Traces: 5 mils wide, 10 mil spacing.</li> </ul>	<ul style="list-style-type: none"> <li>Refer to <a href="#">Section 9.7</a>.</li> </ul>
	<ul style="list-style-type: none"> <li>LAN Max Trace Length ICH3-S to CNR: L = 3" to 9" (0.5" to 3" on card).</li> </ul>	<ul style="list-style-type: none"> <li>To meet timing requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>Stubs due to R-pak CNR/LOM stuffing option should not be present.</li> </ul>	<ul style="list-style-type: none"> <li>To minimize inductance.</li> </ul>
	<ul style="list-style-type: none"> <li>Maximum Trace Lengths: <ul style="list-style-type: none"> <li>ICH3-S to 82562EH: L = 4.5" to 10"</li> <li>82562ET: L = 3.5" to 10"</li> <li>82562EM: L = 3.5" to 10".</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>To meet timing requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>Maximum mismatch between the length of a clock trace and the length of any data trace is 0.5" (clock must be the longest trace).</li> </ul>	<ul style="list-style-type: none"> <li>To meet timing and signal quality requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.</li> </ul>	<ul style="list-style-type: none"> <li>To meet timing and signal quality requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>Keep the total length of each differential pair under 4".</li> </ul>	<ul style="list-style-type: none"> <li>Issues found with traces longer than 4": <ul style="list-style-type: none"> <li>IEEE phy conformance failures</li> <li>excessive EMI and or degraded receive BER.</li> </ul> </li> </ul>
	<ul style="list-style-type: none"> <li>Do not route the transmit differential traces closer than 100 mils to the receive differential traces.</li> </ul>	<ul style="list-style-type: none"> <li>To minimize crosstalk.</li> </ul>
	<ul style="list-style-type: none"> <li>Distance between differential traces and any other signal line must be at least 100 mils. (300 mils recommended).</li> </ul>	<ul style="list-style-type: none"> <li>To minimize crosstalk.</li> </ul>
	<ul style="list-style-type: none"> <li>Route 5 mils on 7 mils for differential pairs (out of LAN phy).</li> </ul>	<ul style="list-style-type: none"> <li>To meet timing and signal quality requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>Differential trace impedance should be controlled to be ~100 <math>\Omega</math>.</li> </ul>	<ul style="list-style-type: none"> <li>To meet timing and signal quality requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, use two 45-degree bends.</li> </ul>	<ul style="list-style-type: none"> <li>To meet timing and signal quality requirements.</li> </ul>
	<ul style="list-style-type: none"> <li>Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.</li> </ul>	<ul style="list-style-type: none"> <li>This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.</li> </ul>
	<ul style="list-style-type: none"> <li>Do not route traces and vias under crystals or oscillators.</li> </ul>	<ul style="list-style-type: none"> <li>This prevents coupling to or from the clock.</li> </ul>
	<ul style="list-style-type: none"> <li>Trace width to height ratio above the ground plane should be between 1:1 and 3:1.</li> </ul>	<ul style="list-style-type: none"> <li>To control trace EMI radiation.</li> </ul>
	<ul style="list-style-type: none"> <li>Traces between decoupling and I/O filter capacitors should be as short and wide as practical.</li> </ul>	<ul style="list-style-type: none"> <li>Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.</li> </ul>

Table 14-3. Intel® ICH3-S Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
<b>LAN Interface (Continued)</b>		
General Guidelines	<ul style="list-style-type: none"> <li>Vias to decoupling capacitors should be sufficiently large in diameter.</li> </ul>	<ul style="list-style-type: none"> <li>To decrease series inductance.</li> </ul>
	<ul style="list-style-type: none"> <li>Isolate I/O signals from high speed signals.</li> </ul>	<ul style="list-style-type: none"> <li>To minimize crosstalk.</li> </ul>
	<ul style="list-style-type: none"> <li>Avoid routing high-speed LAN or Phone line traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar device.</li> </ul>	<ul style="list-style-type: none"> <li>To minimize crosstalk.</li> </ul>
	<ul style="list-style-type: none"> <li>Place the 82562ET/EM part more than 1.5" away from any board edge.</li> </ul>	<ul style="list-style-type: none"> <li>This minimizes the potential for EMI radiation problems.</li> </ul>
	<ul style="list-style-type: none"> <li>Place at least one bulk capacitor (4.7 <math>\mu</math>F or greater OK) on each side of the 82562ET/EM.</li> </ul>	<ul style="list-style-type: none"> <li>Research and development has shown that this is a robust design recommendation.</li> </ul>
	<ul style="list-style-type: none"> <li>Place decoupling capacitors (0.1 <math>\mu</math>F) as close to the 82562ET/EM as possible.</li> </ul>	
<b>Power Decoupling</b>		
V_CPU_IO[2:0]	<ul style="list-style-type: none"> <li>Use one 0.1 <math>\mu</math>F decoupling capacitor. Locate within 100 mils of the ICH3-S processor interface balls.</li> </ul>	<ul style="list-style-type: none"> <li>Used to pull-up all processor I/F signals.</li> </ul>
VCC_3.3	<ul style="list-style-type: none"> <li>Requires six 0.1 <math>\mu</math>F decoupling capacitors. Distribute around the ICH3-S package sides within 100 mils from the package balls:               <ul style="list-style-type: none"> <li>Top near AUX/PCI</li> <li>Left across the PCI and LPC</li> <li>Bottom near IDE.</li> </ul> </li> </ul>	
VCCSUS_3.3	<ul style="list-style-type: none"> <li>Requires two 0.1 <math>\mu</math>F decoupling capacitors. Place one capacitor on the top side within 200 mils of the USB center. Place other on bottom side near the VCCSus3_3 supply.</li> </ul>	
VCC_1.8	<ul style="list-style-type: none"> <li>Requires four 0.1 <math>\mu</math>F decoupling capacitors. Locate two capacitors distributed local to the hub interface; within 50 mils of the package hub interface balls. Distribute remaining capacitors on the left and bottom sides of the package for core delivery.</li> </ul>	
VCCSUS_1.8	<ul style="list-style-type: none"> <li>Requires one 0.1 <math>\mu</math>F decoupling capacitor. Locate within 200 mils of balls B23 and C23 of the ICH3-S.</li> </ul>	
V5_REF_SUS	<ul style="list-style-type: none"> <li>Requires one 0.1 <math>\mu</math>F decoupling capacitor. V5_REF_Sus affects only 5 V-tolerance for USB OC[5:0]# balls, and can be connected to VCCSus3_3 if 5 V tolerance on these signal is not required.</li> </ul>	
V5_REF	<ul style="list-style-type: none"> <li>Requires one 0.1 <math>\mu</math>F decoupling capacitor. V5REF is the reference voltage for 5V tolerant inputs in the ICH3-S. Tie to balls V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.</li> </ul>	

Table 14-3. Intel® ICH3-S Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
<b>RTC</b>		
General Guidelines	<ul style="list-style-type: none"> <li>• RTC LEAD length = 0.25" Max.</li> <li>• Minimize capacitance between RTCX1 and RTCX2.</li> <li>• Put GND plane underneath Crystal components.</li> <li>• Don't route switching signals under the external components (unless on other side of board).</li> </ul>	
<b>USB</b>		
General Guidelines	<ul style="list-style-type: none"> <li>• Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)</li> <li>• Keep traces at least 50 mils away from the edge of the reference ground plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.</li> <li>• Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 <math>\Omega</math> differential impedance. (Recommended: 5 on 6 spacing with 4-layer 4.5 mil prepreg stackup).</li> <li>• Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 20 mils, though it is recommended to keep clocks and PCI traces at least 50 mils from the USB differential pairs if possible.</li> <li>• Use 20 mil minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk.</li> <li>• USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as USBP2P and USBP2N) should be no greater than 150 mils.</li> <li>• No termination resistors needed for USB. ICH3-S has internal 15 k<math>\Omega</math> resistors.</li> <li>• 47 pF parallel capacitors may be placed as close to the USB connector as possible.</li> </ul>	

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# Schematics

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# 15

The E7500 Chipset Customer Reference Board schematics are attached.

**Note:** Due to drawing tool capabilities, there are different representation of the voltage values throughout the schematics. i.e., V3\_3 implies the value of VCC3.3, V2\_5 implies the value of VCC2.5, and so forth.

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# INTEL(R) XEON(TM) PROCESSOR WITH 512KB L2 CACHE AND INTEL(R) E7500 CHIPSET REFERENCE SCHEMATICS

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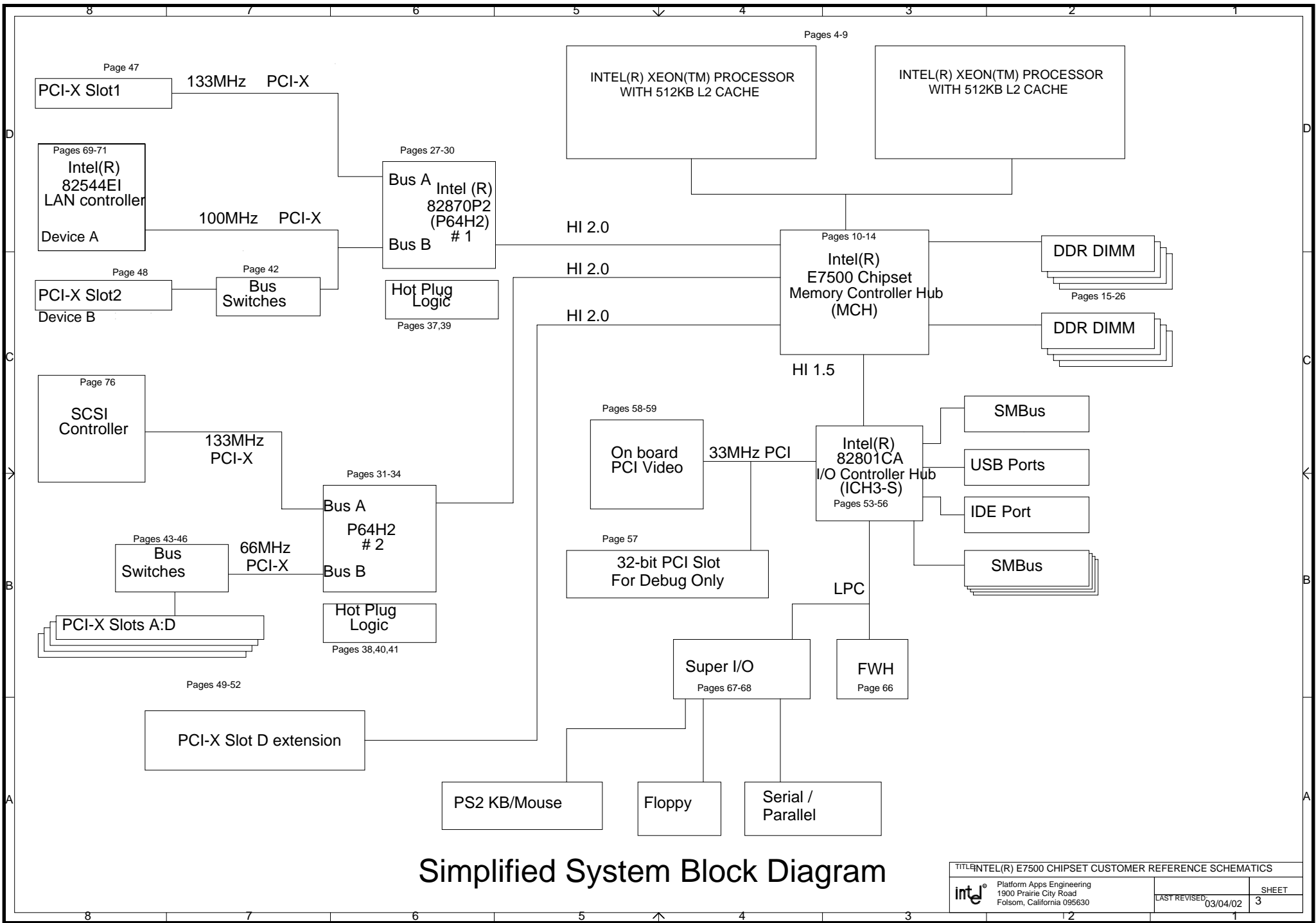
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	Platform Apps Engineering 1900 Prairie City Road Folsom, California 95630	LAST REVISED: 03/04/02
		SHEET 1

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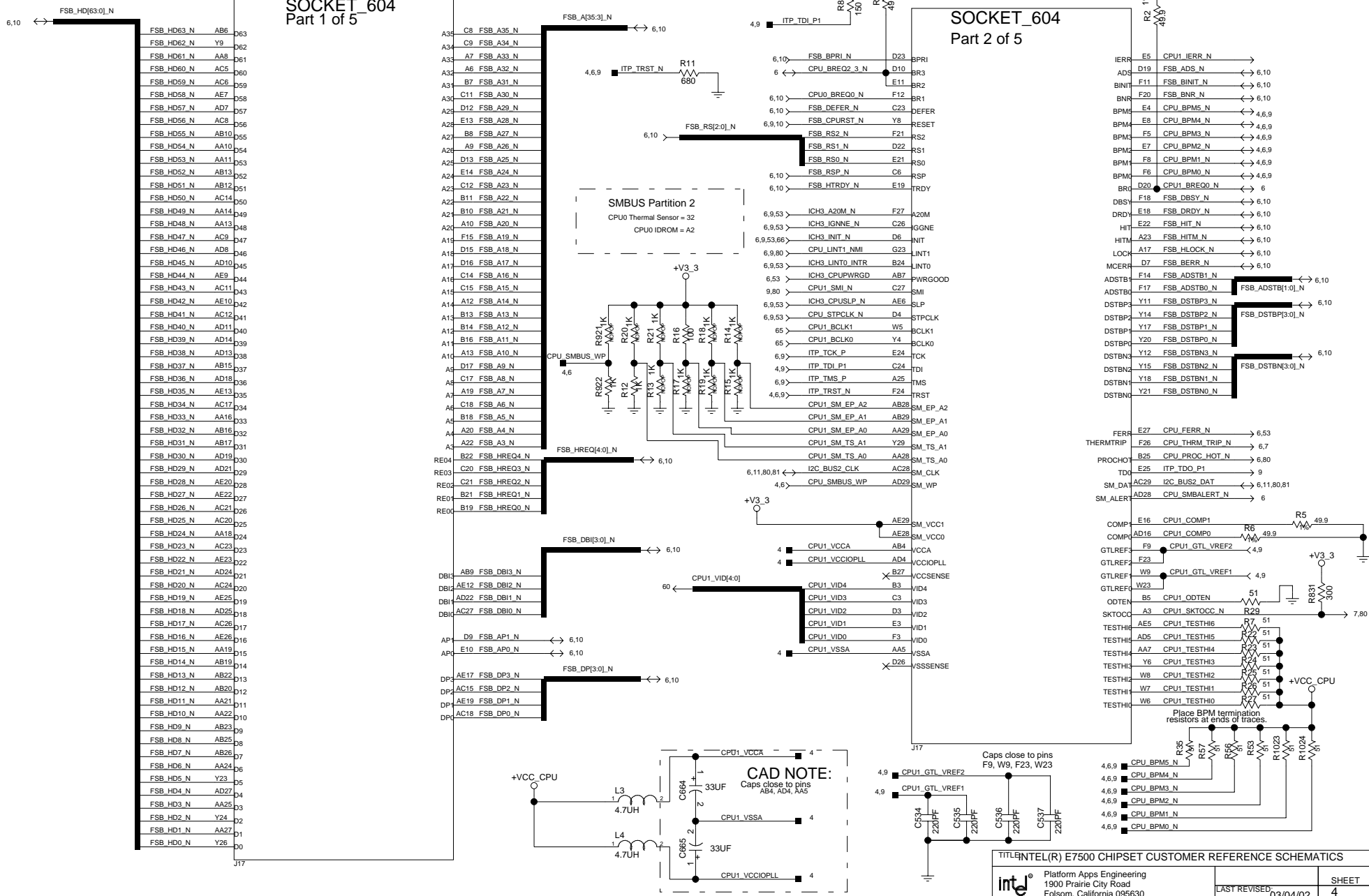


Simplified System Block Diagram

# Processor 1 Connector (Middle processor)

SOCKET\_604  
Part 1 of 5

SOCKET\_604  
Part 2 of 5



# Processor 1 Connector

+VCC\_CPU

+VCC\_CPU

SOCKET\_604  
Part 3 of 5  
VCC Pins

SOCKET\_604  
Part 4 of 5  
VSS Pins

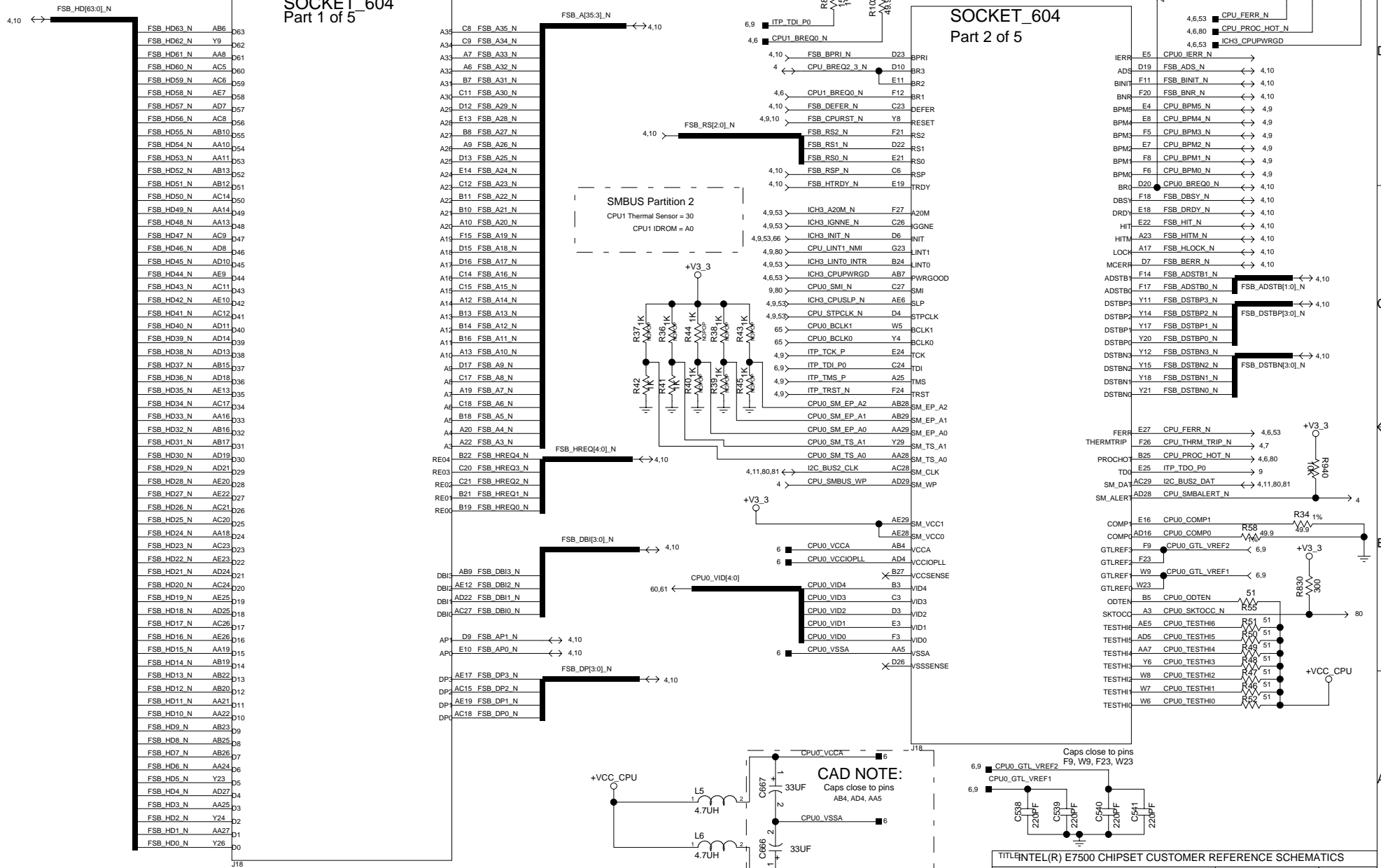
SOCKET\_604  
Part 5 of 5  
Reserved Pins

AC1	RSVD1	AE16
W3	RSVD2	AE15
D25	RSVD3	AE4
C5	RSVD4	AB3
A26	RSVD5	AA3
A16	RSVD6	Y28
A15	RSVD7	Y27
A4	RSVD8	Y3
A1	RSVD9	AD1
AE30	RSVD20	B1

# Processor 0 Connector (End Processor)

SOCKET\_604  
Part 1 of 5

SOCKET\_604  
Part 2 of 5



**Processor 0 Connector**

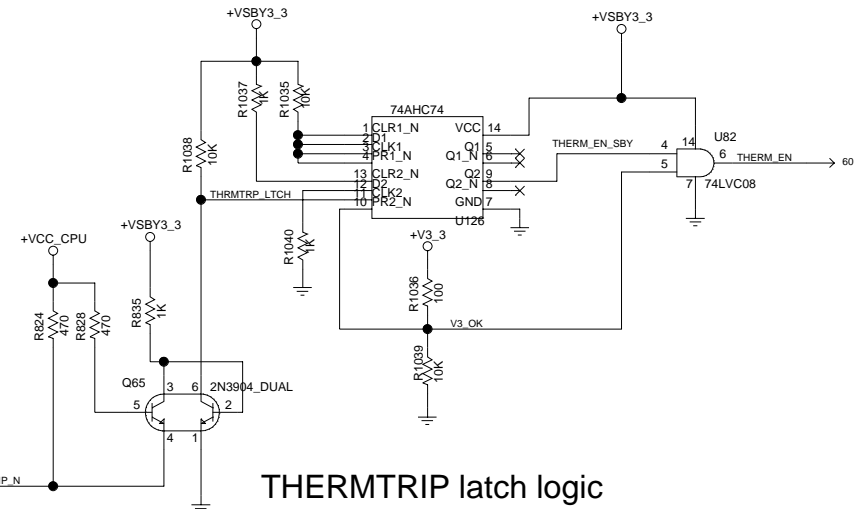
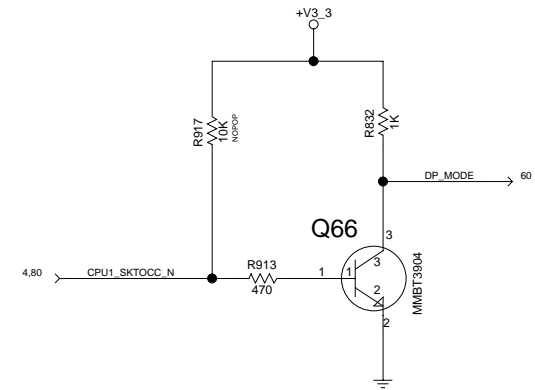
**SOCKET\_604 Part 3 of 5 VCC Pins**

**SOCKET\_604 Part 4 of 5 VSS Pins**

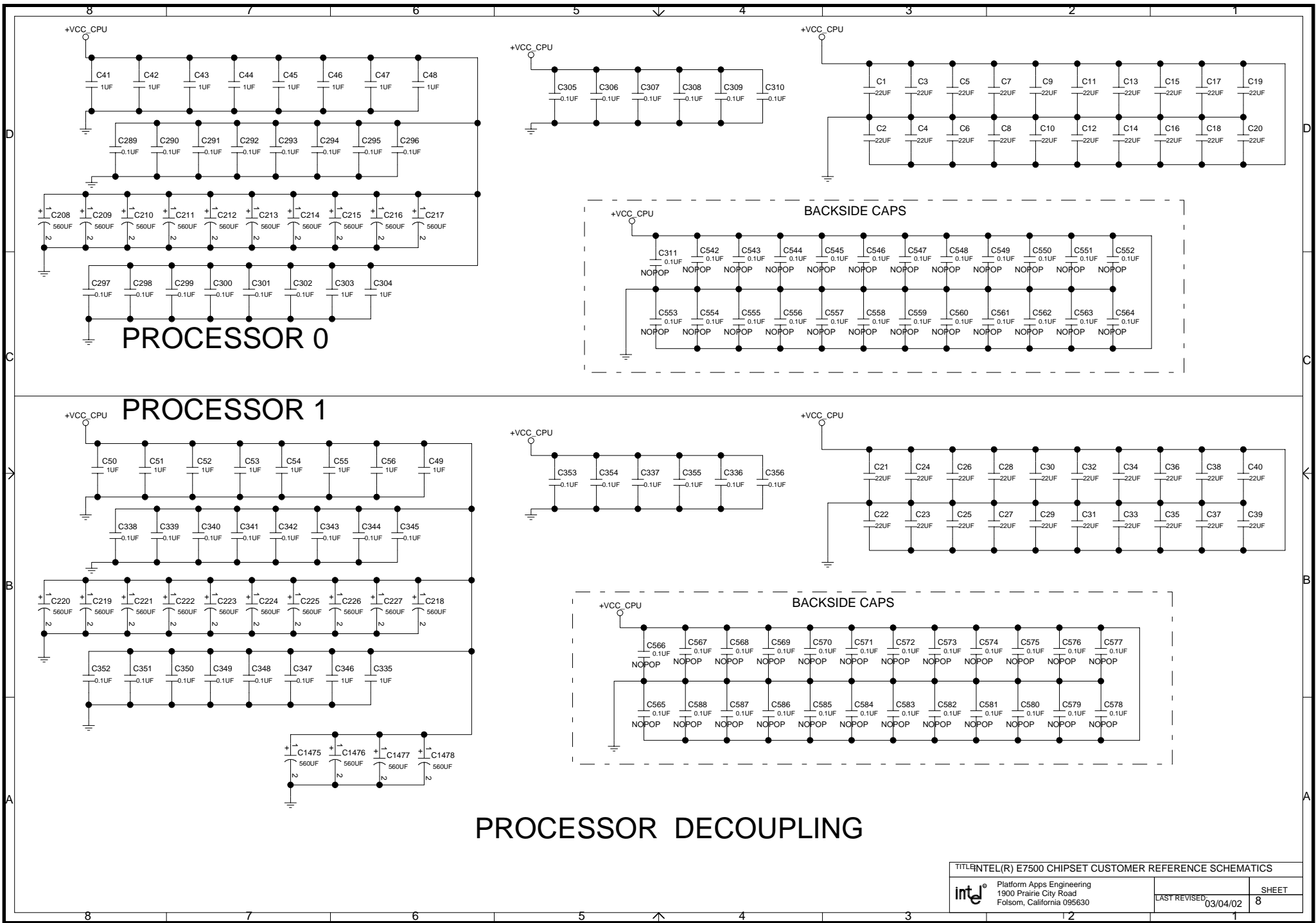
**SOCKET\_604 Part 5 of 5 Reserved Pins**

**THERMTRIP latch logic**

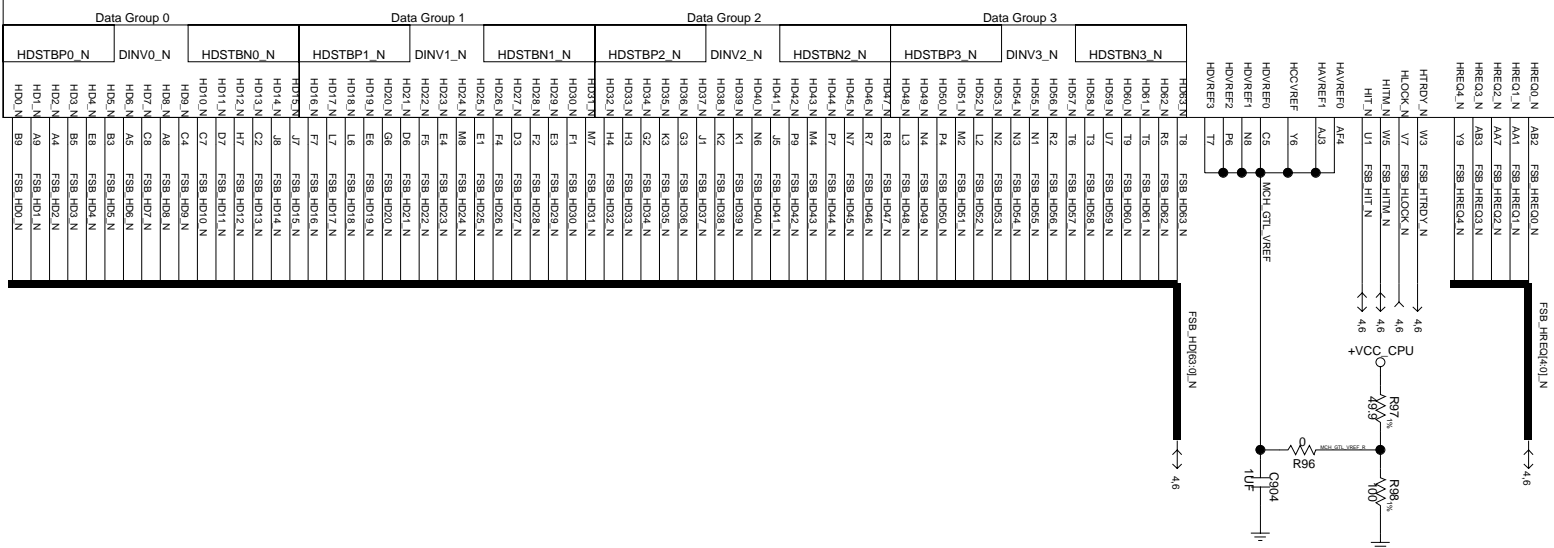
The diagram illustrates the electrical connections for the Processor 0 Connector. It includes three sections of the connector: VCC pins (Part 3 of 5), VSS pins (Part 4 of 5), and reserved pins (Part 5 of 5). The VCC pins are connected to +VCC\_CPU, and the VSS pins are connected to ground. The reserved pins are connected to various signals, including AC1, W3, D25, C5, A26, A16, A15, A4, A1, AE30, AE16, AE15, AE4, AB3, AA3, Y28, Y27, Y3, AD1, and B1. The thermtrip latch logic is shown, featuring a 74AHC74 flip-flop (U2) and a 74VHC08 NAND gate (U126). The logic is triggered by the CPU\_THRM\_TRIP\_N signal and the THERMTRIP\_LATCH signal, and it controls the THERM\_EN\_SBY signal. The diagram also shows the connection of the THERMTRIP\_LATCH signal to the CPU\_THRM\_TRIP\_N signal via a 470 ohm resistor (R824).



## THERMTRIP latch logic







## Memory Controller Hub (MCH)



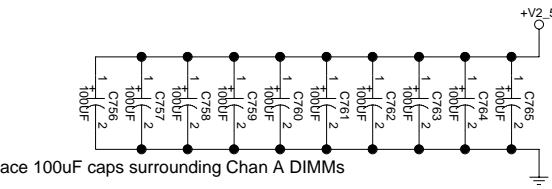





# MCH DDR B

21	↔	DDR8_D00	F33	D00_B	
21	↔	DDR8_D01	K30	D01_B	
21	↔	DDR8_D02	J32	D02_B	
21	↔	DDR8_D03	N26	D03_B	Low Nibble Data Group 0
21	↔	DDR8_D050	L30	D050_B	
21	↔	DDR8_D059	H31	D059_B	
21	↔	DDR8_D04	N27	D04_B	
21	↔	DDR8_D05	G32	D05_B	
21	↔	DDR8_D06	M26	D06_B	High Nibble Data Group 0
21	↔	DDR8_D07	N28	D07_B	
21	↔	DDR8_D08	J33	D08_B	
21	↔	DDR8_D09	K32	D09_B	
21	↔	DDR8_D010	P27	D010_B	Low Nibble Data Group 1
21	↔	DDR8_D011	P26	D011_B	
21	↔	DDR8_D081	M31	D081_B	
21	↔	DDR8_D0510	N28	D0510_B	
21	↔	DDR8_D012	J31	D012_B	
21	↔	DDR8_D013	L31	D013_B	High Nibble Data Group 1
21	↔	DDR8_D014	P28	D014_B	
21	↔	DDR8_D015	P29	D015_B	
21	↔	DDR8_D016	T29	D016_B	
21	↔	DDR8_D017	T30	D017_B	
21	↔	DDR8_D018	U30	D018_B	Low Nibble Data Group 2
21	↔	DDR8_D019	T28	D019_B	
21	↔	DDR8_D052	U33	D052_B	
21	↔	DDR8_D0511	U31	D0511_B	
21	↔	DDR8_D050	P32	D050_B	High Nibble Data Group 2
21	↔	DDR8_D021	T27	D021_B	
21	↔	DDR8_D022	V33	D022_B	
21	↔	DDR8_D023	V31	D023_B	
21	↔	DDR8_D024	P30	D024_B	
21	↔	DDR8_D025	P33	D025_B	Low Nibble Data Group 3
21	↔	DDR8_D026	R28	D026_B	
21	↔	DDR8_D027	T32	D027_B	
21	↔	DDR8_D053	R28	D053_B	
21	↔	DDR8_D0512	R31	D0512_B	
21	↔	DDR8_D028	N32	D028_B	
21	↔	DDR8_D029	P31	D029_B	High Nibble Data Group 3
21	↔	DDR8_D030	R29	D030_B	
21	↔	DDR8_D031	T33	D031_B	
21	↔	DDR8_D032	W27	D032_B	
21	↔	DDR8_D033	A33	D033_B	Low Nibble Data Group 4
21	↔	DDR8_D034	A31	D034_B	
21	↔	DDR8_D035	W21	D035_B	
21	↔	DDR8_D054	A32	D054_B	
21	↔	DDR8_D0513	A30	D0513_B	
21	↔	DDR8_D036	A32	D036_B	High Nibble Data Group 4
21	↔	DDR8_D037	A30	D037_B	
21	↔	DDR8_D038	A33	D038_B	
21	↔	DDR8_D039	W28	D039_B	
21	↔	DDR8_D040	A29	D040_B	
21	↔	DDR8_D041	A33	D041_B	Low Nibble Data Group 5
21	↔	DDR8_D042	V28	D042_B	
21	↔	DDR8_D043	A30	D043_B	
21	↔	DDR8_D055	A31	D055_B	
21	↔	DDR8_D0514	A30	D0514_B	
21	↔	DDR8_D044	V28	D044_B	High Nibble Data Group 5
21	↔	DDR8_D045	A32	D045_B	
21	↔	DDR8_D046	A33	D046_B	
21	↔	DDR8_D047	V28	D047_B	
21	↔	DDR8_D048	V28	D048_B	
21	↔	DDR8_D049	A32	D049_B	Low Nibble Data Group 6
21	↔	DDR8_D050	A32	D050_B	
21	↔	DDR8_D051	A31	D051_B	
21	↔	DDR8_D056	A33	D056_B	
21	↔	DDR8_D0515	A32	D0515_B	
21	↔	DDR8_D052	A32	D052_B	
21	↔	DDR8_D053	A33	D053_B	High Nibble Data Group 6
21	↔	DDR8_D054	A33	D054_B	
21	↔	DDR8_D055	A33	D055_B	
21	↔	DDR8_D056	A33	D056_B	
21	↔	DDR8_D057	A30	D057_B	
21	↔	DDR8_D058	A32	D058_B	Low Nibble Data Group 7
21	↔	DDR8_D059	A33	D059_B	
21	↔	DDR8_D0516	A32	D0516_B	
21	↔	DDR8_D060	A32	D060_B	
21	↔	DDR8_D061	A31	D061_B	High Nibble Data Group 7
21	↔	DDR8_D062	A32	D062_B	
21	↔	DDR8_D063	A33	D063_B	
21	↔	DDR8_D064	A33	D064_B	
21	↔	DDR8_D065	A33	D065_B	
21	↔	DDR8_D066	A30	D066_B	
21	↔	DDR8_D067	A32	D067_B	
21	↔	DDR8_D068	A33	D068_B	Low Nibble Data Group 8
21	↔	DDR8_D069	A33	D069_B	
21	↔	DDR8_D07	A32	D07_B	
21	↔	DDR8_D081	A31	D081_B	
21	↔	DDR8_D082	A32	D082_B	
21	↔	DDR8_D083	A33	D083_B	High Nibble Data Group 8
21	↔	DDR8_D084	A33	D084_B	
21	↔	DDR8_D085	A33	D085_B	
21	↔	DDR8_D086	A33	D086_B	
21	↔	DDR8_D087	A33	D087_B	
21	↔	DDR8_D088	A33	D088_B	
21	↔	DDR8_D089	A33	D089_B	
21	↔	DDR8_D090	A33	D090_B	
21	↔	DDR8_D091	A33	D091_B	
21	↔	DDR8_D092	A33	D092_B	
21	↔	DDR8_D093	A33	D093_B	
21	↔	DDR8_D094	A33	D094_B	
21	↔	DDR8_D095	A33	D095_B	
21	↔	DDR8_D096	A33	D096_B	
21	↔	DDR8_D097	A33	D097_B	
21	↔	DDR8_D098	A33	D098_B	
21	↔	DDR8_D099	A33	D099_B	
21	↔	DDR8_D100	A33	D100_B	
21	↔	DDR8_D101	A33	D101_B	
21	↔	DDR8_D102	A33	D102_B	
21	↔	DDR8_D103	A33	D103_B	
21	↔	DDR8_D104	A33	D104_B	
21	↔	DDR8_D105	A33	D105_B	
21	↔	DDR8_D106	A33	D106_B	
21	↔	DDR8_D107	A33	D107_B	
21	↔	DDR8_D108	A33	D108_B	
21	↔	DDR8_D109	A33	D109_B	
21	↔	DDR8_D110	A33	D110_B	
21	↔	DDR8_D111	A33	D111_B	
21	↔	DDR8_D112	A33	D112_B	
21	↔	DDR8_D113	A33	D113_B	
21	↔	DDR8_D114	A33	D114_B	
21	↔	DDR8_D115	A33	D115_B	
21	↔	DDR8_D116	A33	D116_B	
21	↔	DDR8_D117	A33	D117_B	
21	↔	DDR8_D118	A33	D118_B	
21	↔	DDR8_D119	A33	D119_B	
21	↔	DDR8_D120	A33	D120_B	
21	↔	DDR8_D121	A33	D121_B	
21	↔	DDR8_D122	A33	D122_B	
21	↔	DDR8_D123	A33	D123_B	
21	↔	DDR8_D124	A33	D124_B	
21	↔	DDR8_D125	A33	D125_B	
21	↔	DDR8_D126	A33	D126_B	
21	↔	DDR8_D127	A33	D127_B	
21	↔	DDR8_D128	A33	D128_B	
21	↔	DDR8_D129	A33	D129_B	
21	↔	DDR8_D130	A33	D130_B	
21	↔	DDR8_D131	A33	D131_B	
21	↔	DDR8_D132	A33	D132_B	
21	↔	DDR8_D133	A33	D133_B	
21	↔	DDR8_D134	A33	D134_B	
21	↔	DDR8_D135	A33	D135_B	
21	↔	DDR8_D136	A33	D136_B	
21	↔	DDR8_D137	A33	D137_B	
21	↔	DDR8_D138	A33	D138_B	
21	↔	DDR8_D139	A33	D139_B	
21	↔	DDR8_D140	A33	D140_B	
21	↔	DDR8_D141	A33	D141_B	
21	↔	DDR8_D142	A33	D142_B	
21	↔	DDR8_D143	A33	D143_B	
21	↔	DDR8_D144	A33	D144_B	
21	↔	DDR8_D145	A33	D145_B	
21	↔	DDR8_D146	A33	D146_B	
21	↔	DDR8_D147	A33	D147_B	
21	↔	DDR8_D148	A33	D148_B	
21	↔	DDR8_D149	A33	D149_B	
21	↔	DDR8_D150	A33	D150_B	
21	↔	DDR8_D151	A33	D151_B	
21	↔	DDR8_D152	A33	D152_B	
21	↔	DDR8_D153	A33	D153_B	
21	↔	DDR8_D154	A33	D154_B	
21	↔	DDR8_D155	A33	D155_B	
21	↔	DDR8_D156	A33	D156_B	
21	↔	DDR8_D157	A33	D157_B	
21	↔	DDR8_D158	A33	D158_B	
21	↔	DDR8_D159	A33	D159_B	
21	↔	DDR8_D160	A33	D160_B	
21	↔	DDR8_D161	A33	D161_B	
21	↔	DDR8_D162	A33	D162_B	
21	↔	DDR8_D163	A33	D163_B	
21	↔	DDR8_D164	A33	D164_B	
21	↔	DDR8_D165	A33	D165_B	
21	↔	DDR8_D166	A33	D166_B	
21	↔	DDR8_D167	A33	D167_B	
21	↔	DDR8_D168	A33	D168_B	
21	↔	DDR8_D169	A33	D169_B	
21	↔	DDR8_D170	A33	D170_B	
21	↔	DDR8_D171	A33	D171_B	
21	↔	DDR8_D172	A33	D172_B	
21	↔	DDR8_D173	A33	D173_B	
21	↔	DDR8_D174	A33	D174_B	
21	↔	DDR8_D175	A33	D175_B	
21	↔	DDR8_D176	A33	D176_B	
21	↔	DDR8_D177	A33	D177_B	
21	↔	DDR8_D178	A33	D178_B	
21	↔	DDR8_D179	A33	D179_B	
21	↔	DDR8_D180	A33	D180_B	
21	↔	DDR8_D181	A33	D181_B	
21	↔	DDR8_D182	A33	D182_B	
21	↔	DDR8_D183	A33	D183_B	
21	↔	DDR8_D184	A33	D184_B	
21	↔	DDR8_D185	A33	D185_B	
21	↔	DDR8_D186	A33	D186_B	
21	↔	DDR8_D187	A33	D187_B	
21	↔	DDR8_D188	A33	D188_B	
21	↔	DDR8_D189	A33	D189_B	
21	↔	DDR8_D190	A33	D190_B	
21	↔	DDR8_D191	A33	D191_B	
21	↔	DDR8_D192	A33	D192_B	
21	↔	DDR8_D193	A33	D193_B	
21	↔	DDR8_D194	A33	D194_B	
21	↔	DDR8_D195	A33	D195_B	
21	↔	DDR8_D196	A33	D196_B	
21	↔	DDR8_D197	A33	D197_B	
21	↔	DDR8_D198	A33	D198_B	
21	↔	DDR8_D199	A33	D199_B	
21	↔	DDR8_D200	A33	D200_B	
21	↔	DDR8_D201	A33	D201_B	
21	↔	DDR8_D202	A33	D202_B	
21	↔	DDR8_D203	A33	D203_B	
21	↔	DDR8_D204	A33	D204_B	
21	↔	DDR8_D205	A33	D205_B	
21	↔	DDR8_D206	A33	D206_B	
21	↔	DDR8_D207	A33	D207_B	
21	↔	DDR8_D208	A33	D208_B	
21	↔	DDR8_D209	A33	D209_B	
21	↔	DDR8_D210	A33	D210_B	
21	↔	DDR8_D211	A33	D211_B	
21	↔	DDR8_D212	A33	D212_B	
21	↔	DDR8_D213	A33	D213_B	
21	↔	DDR8_D214	A33	D214_B	
21	↔	DDR8_D215	A33	D215_B	
21	↔	DDR8_D216	A33	D216_B	
21	↔	DDR8_D217	A33	D217_B	
21	↔	DDR8_D218	A33	D218_B	
21	↔	DDR8_D219	A33	D219_B	
21	↔	DDR8_D220	A33	D220_B	
21	↔	DDR8_D221	A33	D221_B	
21	↔	DDR8_D222	A33	D222_B	
21	↔	DDR8_D223	A33	D223_B	
21	↔	DDR8_D224	A33	D224_B	
21	↔	DDR8_D225	A33	D225_B	
21	↔	DDR8_D226	A33	D226_B	
21	↔	DDR8_D227	A33	D227_B	
21	↔	DDR8_D228	A33	D228_B	
21	↔	DDR8_D229	A33	D229_B	
21	↔	DDR8_D230	A33	D230_B	
21	↔	DDR8_D231	A33	D231_B	
21	↔	DDR8_D232	A33	D232_B	
21	↔	DDR8_D233	A33	D233_B	
21	↔	DDR8_D234	A33	D234_B	
21	↔	DDR8_D235	A33	D235_B	
21	↔	DDR8_D236	A33	D236_B	
21	↔	DDR8_D237	A33	D237_B	
21	↔	DDR8			

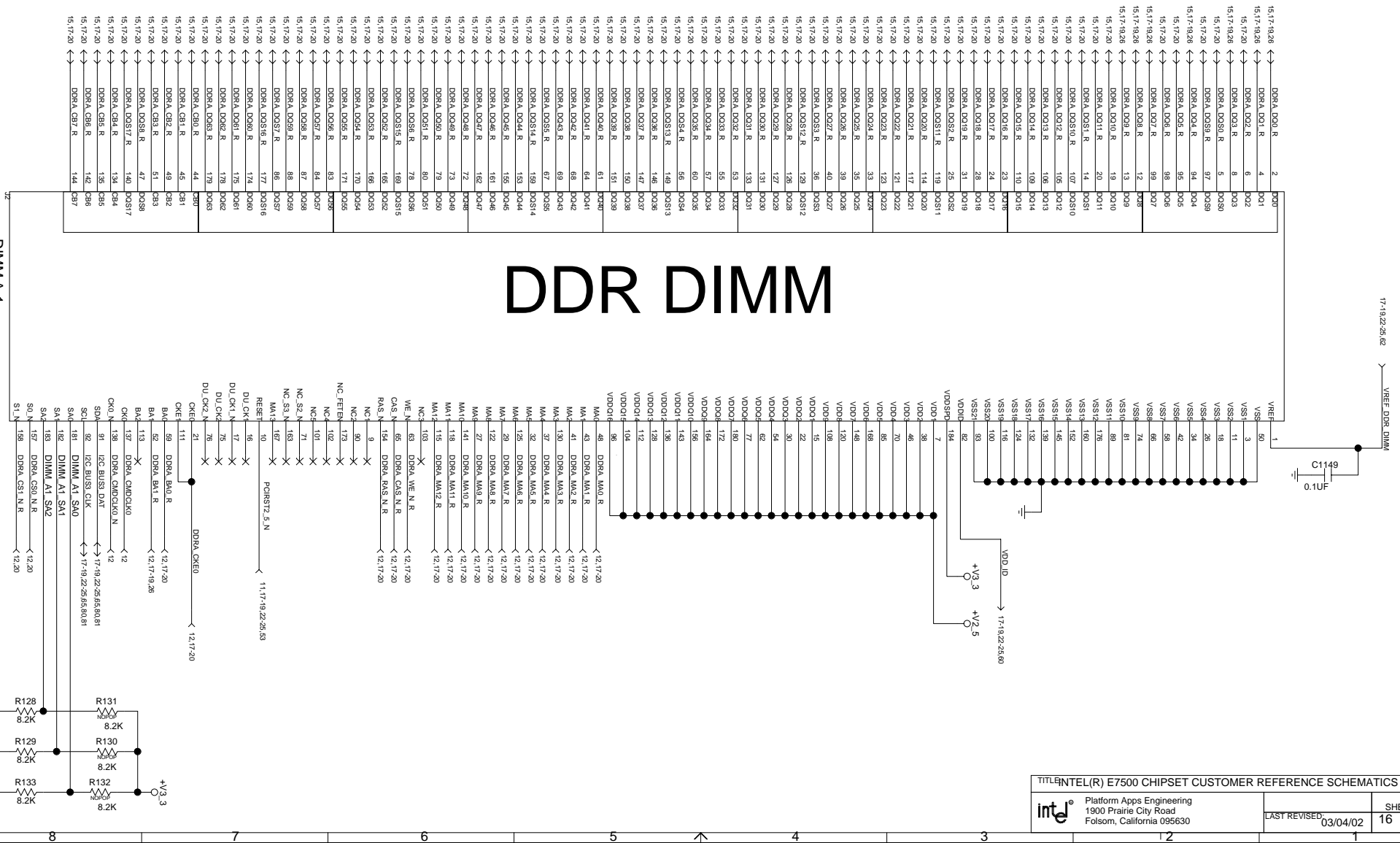


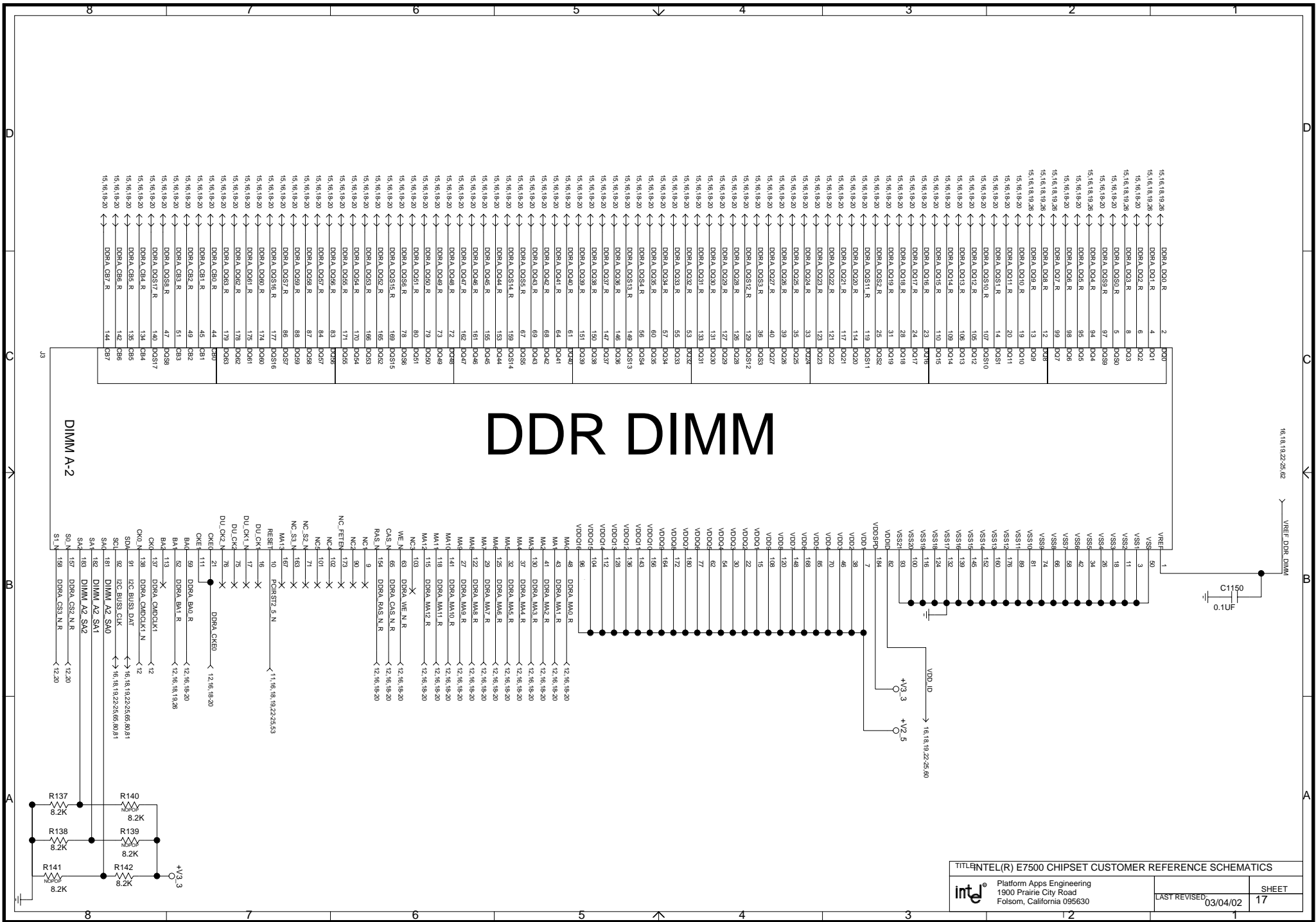
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 Platform Apps Engineering 1900 Prairie City Road Folsom, California 095630			SHEET
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## Place DIMM A-1 Closest to MCH

# DDR DIMM





16,17,18,22,24,62

✓ VREF\_DDR\_DIMM

C1151  
0.1uF

VDD ID → 16,17,19,22,25,60

+V3.3 +V2.5

INTEL(R) E7500 CHIPSET CUSTOMER REFERENCE SCHEMATICS

Platform Apps Engineering  
1900 Prairie City Road  
Folsom, California 95630

LAST REVISED 03/04/02

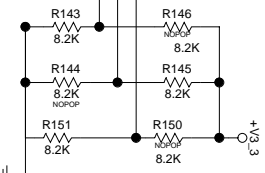
SHEET 18

# DDR DIMM

15-17,18,26 ↔	DDR6, DD0 R	2	DD0
15-17,18,26 ↔	DDR6, DD1 R	4	DD1
15-17,19,20 ↔	DDR6, DD2 R	6	DD2
15-17,18,26 ↔	DDR6, DD3 R	8	DD3
15-17,18,20 ↔	DDR6, DD39 R	5	DD39
15-17,18,20 ↔	DDR6, DD39 R	97	DD39
15-17,18,26 ↔	DDR6, DD4 R	64	DD4
15-17,18,20 ↔	DDR6, DD6 R	86	DD6
15-17,18,20 ↔	DDR6, DD6 R	96	DD6
15-17,18,26 ↔	DDR6, DD7 R	98	DD7
15-17,18,26 ↔	DDR6, DD8 R	12	DD8
15-17,18,26 ↔	DDR6, DD9 R	13	DD9
15-17,18,20 ↔	DDR6, DD10 R	16	DD10
15-17,18,20 ↔	DDR6, DD11 R	20	DD11
15-17,18,20 ↔	DDR6, DD31 R	14	DD31
15-17,18,20 ↔	DDR6, DD310 R	107	DD310
15-17,18,20 ↔	DDR6, DD12 R	105	DD12
15-17,18,20 ↔	DDR6, DD13 R	106	DD13
15-17,18,20 ↔	DDR6, DD14 R	109	DD14
15-17,18,20 ↔	DDR6, DD15 R	110	DD15
15-17,18,20 ↔	DDR6, DD16 R	20	DD16
15-17,18,20 ↔	DDR6, DD17 R	24	DD17
15-17,18,20 ↔	DDR6, DD18 R	28	DD18
15-17,18,20 ↔	DDR6, DD19 R	31	DD19
15-17,18,20 ↔	DDR6, DD32 R	26	DD32
15-17,18,20 ↔	DDR6, DD311 R	119	DD311
15-17,18,20 ↔	DDR6, DD20 R	114	DD20
15-17,18,20 ↔	DDR6, DD21 R	117	DD21
15-17,18,20 ↔	DDR6, DD22 R	121	DD22
15-17,18,20 ↔	DDR6, DD23 R	123	DD23
15-17,18,20 ↔	DDR6, DD24 R	30	DD24
15-17,18,20 ↔	DDR6, DD25 R	36	DD25
15-17,18,20 ↔	DDR6, DD26 R	39	DD26
15-17,18,20 ↔	DDR6, DD27 R	40	DD27
15-17,18,20 ↔	DDR6, DD33 R	36	DD33
15-17,18,20 ↔	DDR6, DD312 R	129	DD312
15-17,18,20 ↔	DDR6, DD28 R	126	DD28
15-17,18,20 ↔	DDR6, DD29 R	127	DD29
15-17,18,20 ↔	DDR6, DD30 R	131	DD30
15-17,18,20 ↔	DDR6, DD31 R	133	DD31
15-17,18,20 ↔	DDR6, DD32 R	50	DD32
15-17,18,20 ↔	DDR6, DD33 R	56	DD33
15-17,18,20 ↔	DDR6, DD34 R	57	DD34
15-17,18,20 ↔	DDR6, DD35 R	60	DD35
15-17,18,20 ↔	DDR6, DD36 R	66	DD36
15-17,18,20 ↔	DDR6, DD313 R	149	DD313
15-17,18,20 ↔	DDR6, DD38 R	146	DD38
15-17,18,20 ↔	DDR6, DD37 R	147	DD37
15-17,18,20 ↔	DDR6, DD38 R	150	DD38
15-17,18,20 ↔	DDR6, DD39 R	151	DD39
15-17,18,20 ↔	DDR6, DD40 R	61	DD40
15-17,18,20 ↔	DDR6, DD41 R	64	DD41
15-17,18,20 ↔	DDR6, DD42 R	66	DD42
15-17,18,20 ↔	DDR6, DD43 R	69	DD43
15-17,18,20 ↔	DDR6, DD35 R	67	DD35
15-17,18,20 ↔	DDR6, DD314 R	159	DD314
15-17,18,20 ↔	DDR6, DD44 R	153	DD44
15-17,18,20 ↔	DDR6, DD45 R	155	DD45
15-17,18,20 ↔	DDR6, DD46 R	161	DD46
15-17,18,20 ↔	DDR6, DD47 R	162	DD47
15-17,18,20 ↔	DDR6, DD48 R	72	DD48
15-17,18,20 ↔	DDR6, DD49 R	73	DD49
15-17,18,20 ↔	DDR6, DD50 R	79	DD50
15-17,18,20 ↔	DDR6, DD51 R	80	DD51
15-17,18,20 ↔	DDR6, DD52 R	78	DD52
15-17,18,20 ↔	DDR6, DD515 R	169	DD515
15-17,18,20 ↔	DDR6, DD52 R	165	DD52
15-17,18,20 ↔	DDR6, DD53 R	166	DD53
15-17,18,20 ↔	DDR6, DD54 R	170	DD54
15-17,18,20 ↔	DDR6, DD55 R	171	DD55
15-17,18,20 ↔	DDR6, DD56 R	83	DD56
15-17,18,20 ↔	DDR6, DD57 R	84	DD57
15-17,18,20 ↔	DDR6, DD58 R	87	DD58
15-17,18,20 ↔	DDR6, DD59 R	88	DD59
15-17,18,20 ↔	DDR6, DD59 R	86	DD57
15-17,18,20 ↔	DDR6, DD516 R	177	DD516
15-17,18,20 ↔	DDR6, DD59 R	174	DD59
15-17,18,20 ↔	DDR6, DD61 R	175	DD61
15-17,18,20 ↔	DDR6, DD62 R	178	DD62
15-17,18,20 ↔	DDR6, DD63 R	179	DD63
15-17,18,20 ↔	DDR6, DD64 R	44	DD64
15-17,18,20 ↔	DDR6, DD65 R	46	DD65
15-17,18,20 ↔	DDR6, DD66 R	48	DD66
15-17,18,20 ↔	DDR6, DD67 R	51	DD67
15-17,18,20 ↔	DDR6, DD68 R	47	DD68
15-17,18,20 ↔	DDR6, DD69 R	140	DD69
15-17,18,20 ↔	DDR6, DD70 R	134	DD70
15-17,18,20 ↔	DDR6, DD71 R	135	DD71
15-17,18,20 ↔	DDR6, DD72 R	142	DD72
15-17,18,20 ↔	DDR6, DD73 R	144	DD73

DIMM A-3

MA0	48	DDR6, MA0 R	↔ 12,16,17,19,20
MA1	43	DDR6, MA1 R	↔ 12,16,17,19,20
MA2	41	DDR6, MA2 R	↔ 12,16,17,19,20
MA3	130	DDR6, MA3 R	↔ 12,16,17,19,20
MA4	37	DDR6, MA4 R	↔ 12,16,17,19,20
MA5	32	DDR6, MA5 R	↔ 12,16,17,19,20
MA6	125	DDR6, MA6 R	↔ 12,16,17,19,20
MA7	29	DDR6, MA7 R	↔ 12,16,17,19,20
MA8	122	DDR6, MA8 R	↔ 12,16,17,19,20
MA9	27	DDR6, MA9 R	↔ 12,16,17,19,20
MA10	141	DDR6, MA10 R	↔ 12,16,17,19,20
MA11	118	DDR6, MA11 R	↔ 12,16,17,19,20
MA12	115	DDR6, MA12 R	↔ 12,16,17,19,20
MA13	103	DDR6, MA13 R	↔ 12,16,17,19,20
WE N	63	DDR6, WE N R	↔ 12,16,17,19,20
CSA N	65	DDR6, CSA N R	↔ 12,16,17,19,20
RAS N	154	DDR6, RAS N R	↔ 12,16,17,19,20
NC-3	9		
NC-4	90		
NC-5	173		
NC-6	102		
NC-7	101		
NC-8	71		
NC-9	163		
MA13	167		
RESSET	10	DDR6, RESSET 5 N	↔ 11,16,17,18,22,25,60
DU CK1 N	16		
DU CK1 N	17		
DU CK2 N	75		
DU CK2 N	76		
CKE1	21	DDR6, CKE1	↔ 12,16,17,19,20
CKE2	59	DDR6, CKE2	↔ 12,16,17,19,20
BA1	52	DDR6, BA1 R	↔ 12,16,17,19,20
BA2	113		
CK1	137	DDR6, CK1	↔ 12
CK2	138	DDR6, CK2	↔ 12
SD1	91	DDR6, SD1	↔ 16,17,19,22,25,60,81
SD2	92	DDR6, SD2	↔ 16,17,19,22,25,60,81
SA1	181	DIMM A3 SA1	
SA2	182	DIMM A3 SA2	
SN1	157	DDR6, SN1 N R	↔ 12,26
SN2	158	DDR6, SN2 N R	↔ 12,26





16-18,22-26,62

VREF DDR DIMM

C1152  
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VDD ID 16-18,22-26,60

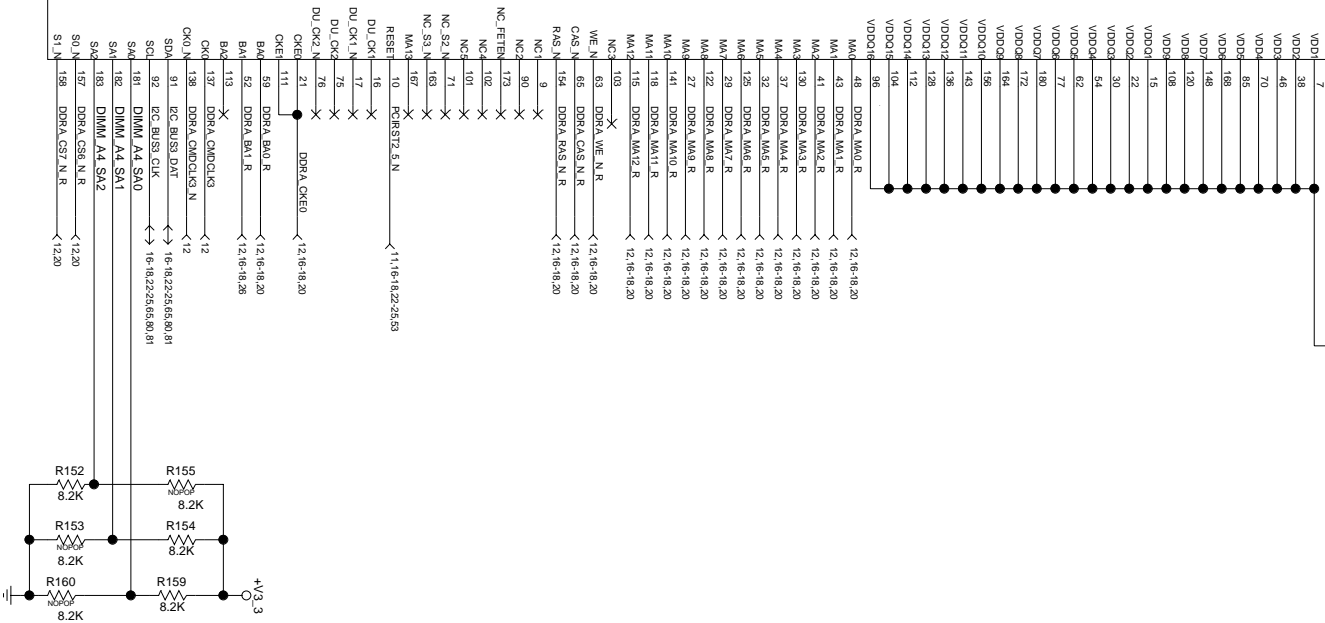
+V3.3

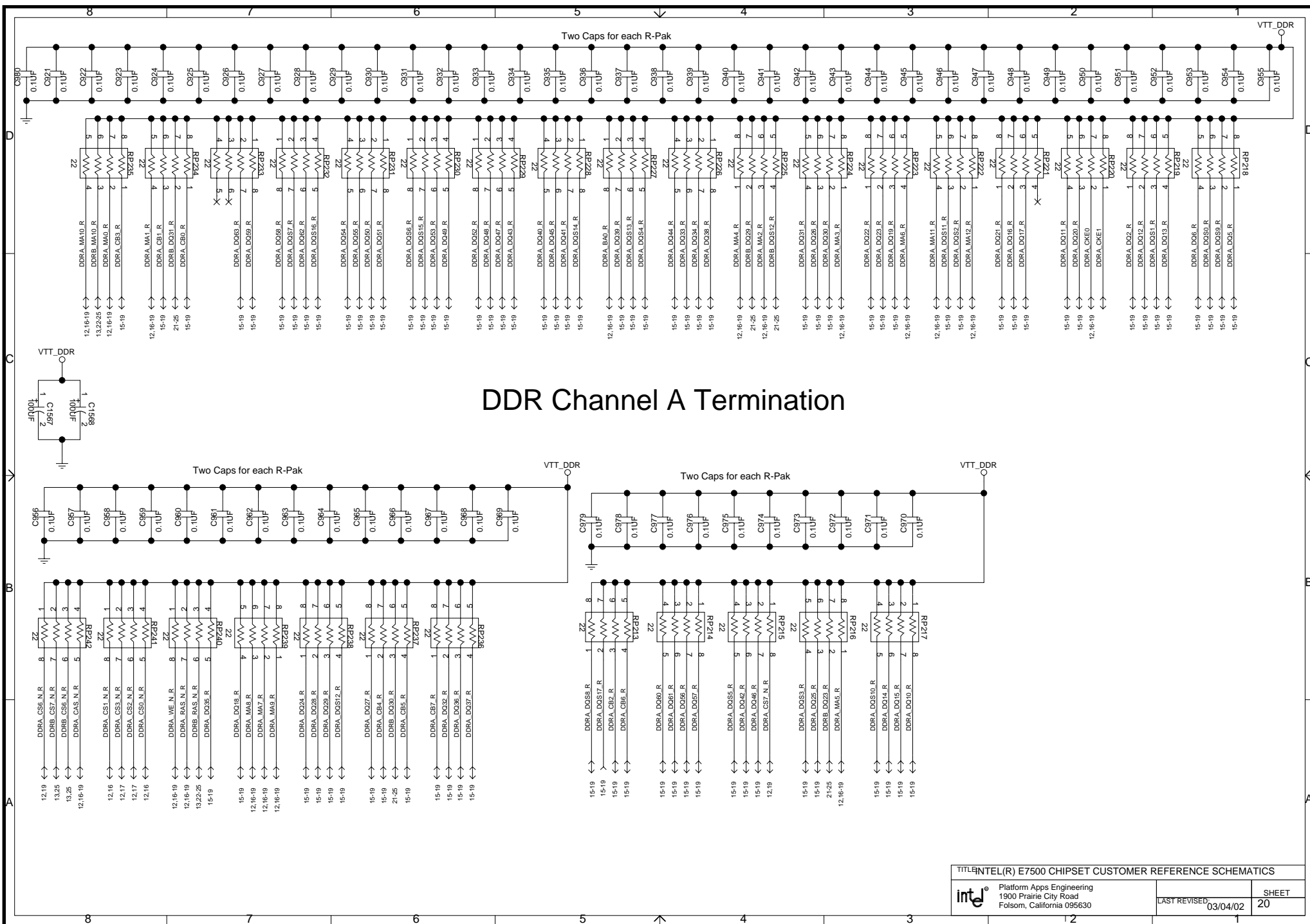
+V2.5

15-18,26	↔	DDR4 D00 R	2	D00
15-18,26	↔	DDR4 D01 R	4	D01
15-18,20	↔	DDR4 D02 R	6	D02
15-18,26	↔	DDR4 D03 R	8	D03
15-18,20	↔	DDR4 D050 R	5	D050
15-18,20	↔	DDR4 D059 R	97	D059
15-18,26	↔	DDR4 D04 R	94	D04
15-18,20	↔	DDR4 D05 R	95	D05
15-18,20	↔	DDR4 D06 R	96	D06
15-18,26	↔	DDR4 D07 R	98	D07
15-18,26	↔	DDR4 D08 R	12	D08
15-18,26	↔	DDR4 D09 R	13	D09
15-18,20	↔	DDR4 D010 R	19	D010
15-18,20	↔	DDR4 D011 R	20	D011
15-18,20	↔	DDR4 D051 R	14	D051
15-18,20	↔	DDR4 D0510 R	107	D0510
15-18,20	↔	DDR4 D012 R	106	D012
15-18,20	↔	DDR4 D013 R	106	D013
15-18,20	↔	DDR4 D014 R	109	D014
15-18,20	↔	DDR4 D015 R	110	D015
15-18,20	↔	DDR4 D016 R	23	D016
15-18,20	↔	DDR4 D017 R	24	D017
15-18,20	↔	DDR4 D018 R	26	D018
15-18,20	↔	DDR4 D019 R	31	D019
15-18,20	↔	DDR4 D052 R	28	D052
15-18,20	↔	DDR4 D0511 R	119	D0511
15-18,20	↔	DDR4 D020 R	114	D020
15-18,20	↔	DDR4 D021 R	117	D021
15-18,20	↔	DDR4 D022 R	121	D022
15-18,20	↔	DDR4 D023 R	123	D023
15-18,20	↔	DDR4 D024 R	33	D024
15-18,20	↔	DDR4 D025 R	35	D025
15-18,20	↔	DDR4 D026 R	39	D026
15-18,20	↔	DDR4 D027 R	40	D027
15-18,20	↔	DDR4 D053 R	36	D053
15-18,20	↔	DDR4 D0512 R	129	D0512
15-18,20	↔	DDR4 D028 R	126	D028
15-18,20	↔	DDR4 D029 R	127	D029
15-18,20	↔	DDR4 D030 R	131	D030
15-18,20	↔	DDR4 D031 R	133	D031
15-18,20	↔	DDR4 D032 R	53	D032
15-18,20	↔	DDR4 D033 R	55	D033
15-18,20	↔	DDR4 D034 R	57	D034
15-18,20	↔	DDR4 D035 R	60	D035
15-18,20	↔	DDR4 D054 R	56	D054
15-18,20	↔	DDR4 D0513 R	146	D0513
15-18,20	↔	DDR4 D036 R	146	D036
15-18,20	↔	DDR4 D037 R	147	D037
15-18,20	↔	DDR4 D038 R	150	D038
15-18,20	↔	DDR4 D039 R	151	D039
15-18,20	↔	DDR4 D040 R	61	D040
15-18,20	↔	DDR4 D041 R	64	D041
15-18,20	↔	DDR4 D042 R	68	D042
15-18,20	↔	DDR4 D043 R	69	D043
15-18,20	↔	DDR4 D055 R	67	D055
15-18,20	↔	DDR4 D0514 R	159	D0514
15-18,20	↔	DDR4 D044 R	153	D044
15-18,20	↔	DDR4 D045 R	155	D045
15-18,20	↔	DDR4 D046 R	161	D046
15-18,20	↔	DDR4 D047 R	162	D047
15-18,20	↔	DDR4 D048 R	72	D048
15-18,20	↔	DDR4 D049 R	73	D049
15-18,20	↔	DDR4 D050 R	79	D050
15-18,20	↔	DDR4 D051 R	80	D051
15-18,20	↔	DDR4 D056 R	78	D056
15-18,20	↔	DDR4 D0515 R	169	D0515
15-18,20	↔	DDR4 D052 R	165	D052
15-18,20	↔	DDR4 D053 R	166	D053
15-18,20	↔	DDR4 D054 R	170	D054
15-18,20	↔	DDR4 D056 R	171	D056
15-18,20	↔	DDR4 D057 R	83	D057
15-18,20	↔	DDR4 D058 R	84	D058
15-18,20	↔	DDR4 D059 R	87	D059
15-18,20	↔	DDR4 D055 R	88	D055
15-18,20	↔	DDR4 D057 R	86	D057
15-18,20	↔	DDR4 D0516 R	177	D0516
15-18,20	↔	DDR4 D060 R	174	D060
15-18,20	↔	DDR4 D061 R	175	D061
15-18,20	↔	DDR4 D062 R	178	D062
15-18,20	↔	DDR4 D063 R	179	D063
15-18,20	↔	DDR4 C00 R	44	C00
15-18,20	↔	DDR4 C01 R	45	C01
15-18,20	↔	DDR4 C02 R	48	C02
15-18,20	↔	DDR4 C03 R	51	C03
15-18,20	↔	DDR4 C051 R	47	C051
15-18,20	↔	DDR4 C04 R	134	C04
15-18,20	↔	DDR4 C05 R	136	C05
15-18,20	↔	DDR4 C06 R	142	C06
15-18,20	↔	DDR4 C07 R	144	C07

# DDR DIMM

DIMM A-4





## D



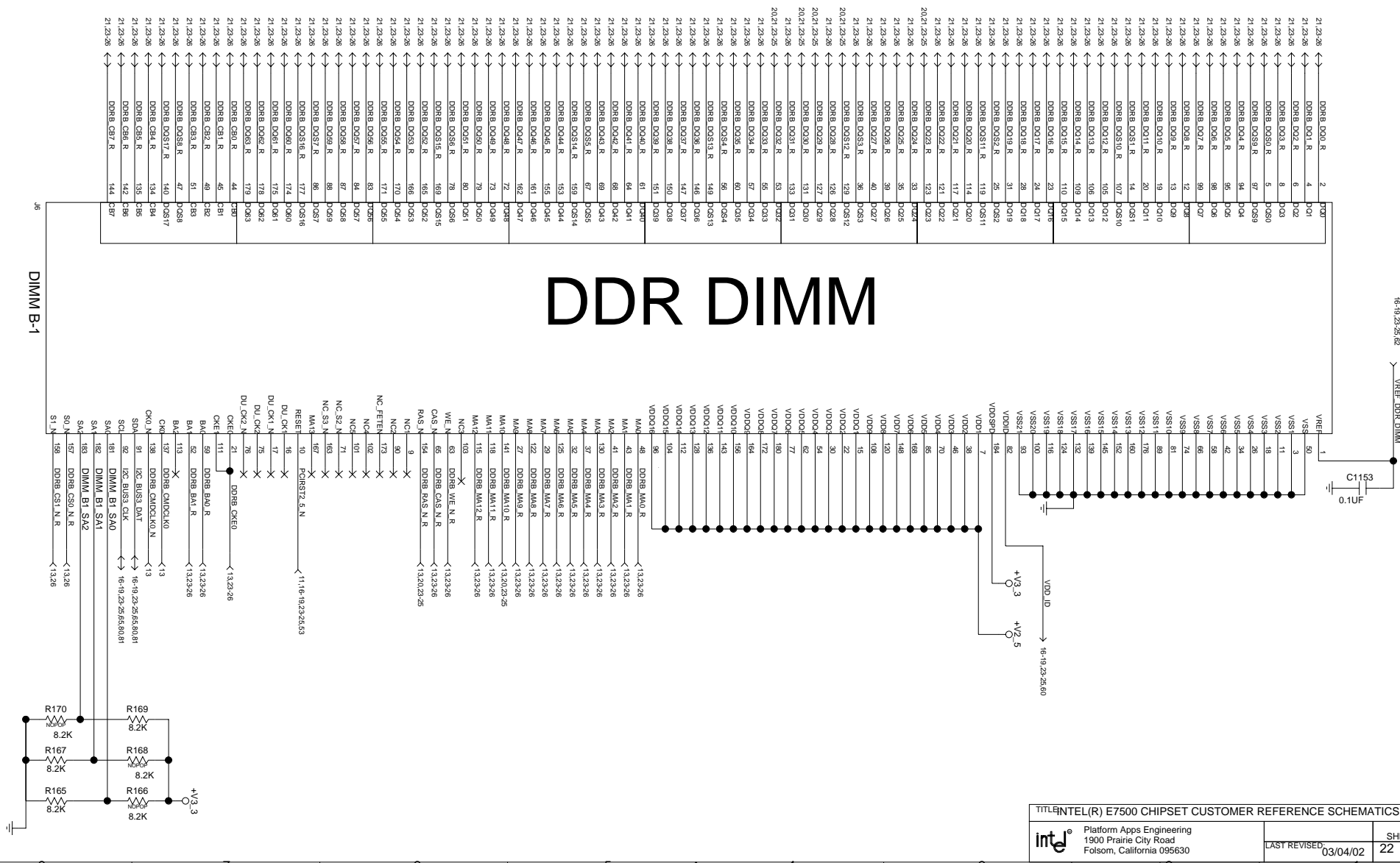
A



A

Place DIMM B-1 Closest to MCH

# DDR DIMM



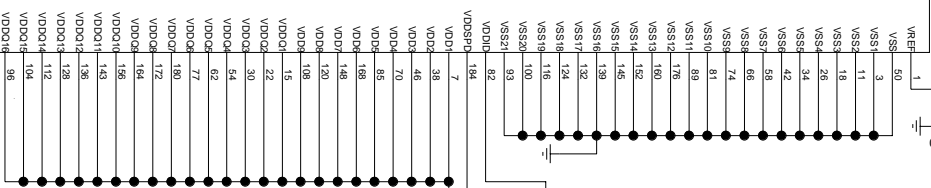
16-19,22,24,25,62

VREF DDR DIMM

C1154  
0.1UF

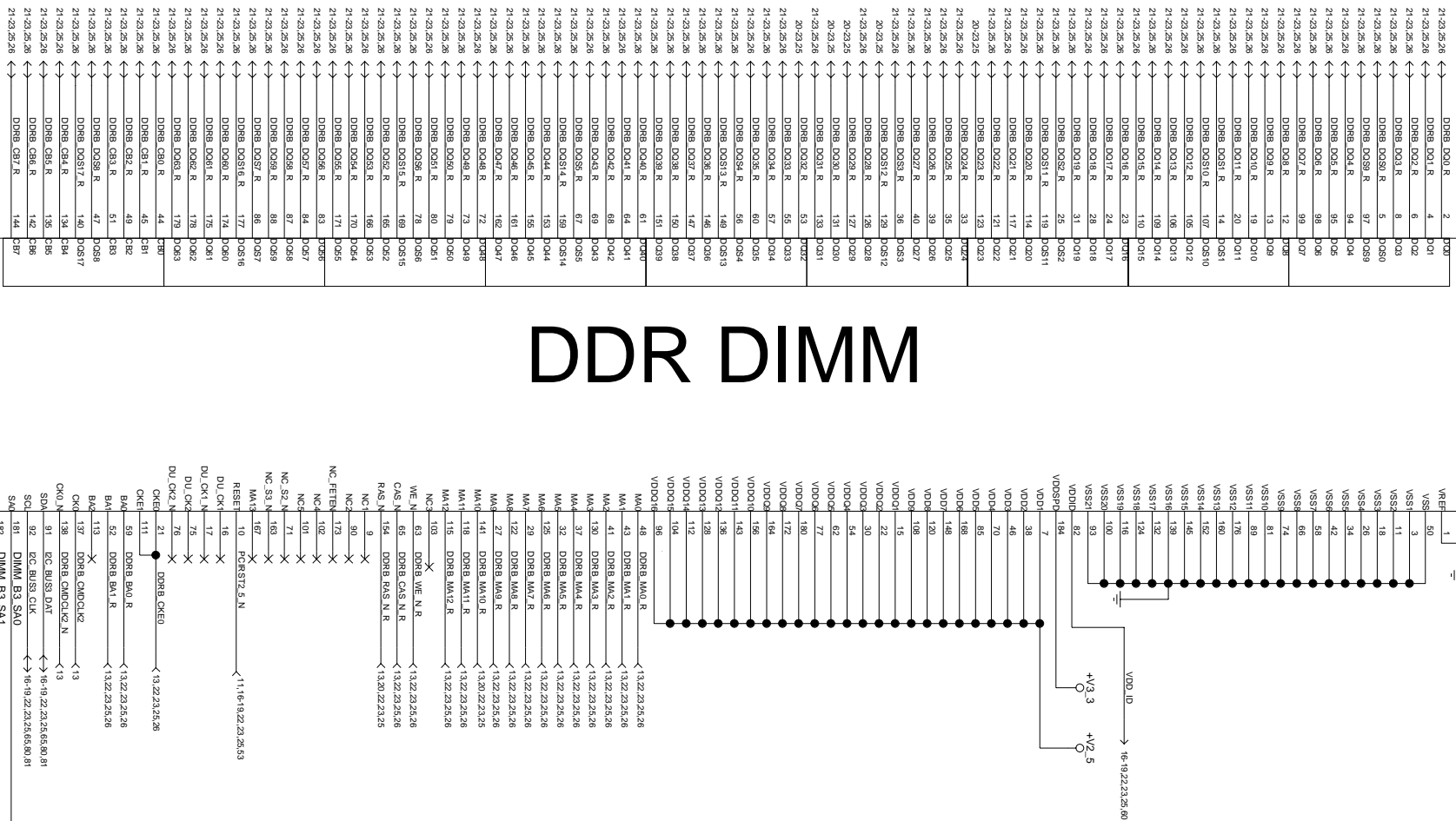
VDD ID 16-19,22,24,25,60

+V3.3  
+V2.5



# DDR DIMM

2122,24,26	↔	DDR8, DQ1, R	2	P01
2122,24,26	↔	DDR8, DQ2, R	4	P02
2122,24,26	↔	DDR8, DQ3, R	6	P03
2122,24,26	↔	DDR8, DQ3, R	5	P050
2122,24,26	↔	DDR8, DQ39, R	5	P050
2122,24,26	↔	DDR8, DQ4, R	97	P059
2122,24,26	↔	DDR8, DQ5, R	94	P04
2122,24,26	↔	DDR8, DQ6, R	95	P05
2122,24,26	↔	DDR8, DQ7, R	98	P06
2122,24,26	↔	DDR8, DQ8, R	12	P08
2122,24,26	↔	DDR8, DQ9, R	13	P09
2122,24,26	↔	DDR8, DQ10, R	19	P010
2122,24,26	↔	DDR8, DQ11, R	20	P011
2122,24,26	↔	DDR8, DQ51, R	14	P051
2122,24,26	↔	DDR8, DQ50, R	107	P0510
2122,24,26	↔	DDR8, DQ52, R	106	P012
2122,24,26	↔	DDR8, DQ53, R	108	P013
2122,24,26	↔	DDR8, DQ54, R	109	P014
2122,24,26	↔	DDR8, DQ55, R	110	P015
2122,24,26	↔	DDR8, DQ56, R	23	P016
2122,24,26	↔	DDR8, DQ57, R	24	P017
2122,24,26	↔	DDR8, DQ58, R	28	P018
2122,24,26	↔	DDR8, DQ59, R	31	P019
2122,24,26	↔	DDR8, DQ60, R	25	P052
2122,24,26	↔	DDR8, DQ61, R	119	P0511
2122,24,26	↔	DDR8, DQ62, R	114	P050
2122,24,26	↔	DDR8, DQ63, R	117	P021
2122,24,26	↔	DDR8, DQ64, R	121	P022
2122,24,26	↔	DDR8, DQ65, R	123	P023
2122,24,26	↔	DDR8, DQ66, R	33	P024
2122,24,26	↔	DDR8, DQ67, R	35	P025
2122,24,26	↔	DDR8, DQ68, R	39	P026
2122,24,26	↔	DDR8, DQ69, R	40	P027
2122,24,26	↔	DDR8, DQ70, R	36	P053
2122,24,26	↔	DDR8, DQ71, R	129	P0512
2052,24,25	↔	DDR8, DQ72, R	127	P029
2052,24,25	↔	DDR8, DQ73, R	131	P030
2052,24,25	↔	DDR8, DQ74, R	133	P031
2052,24,25	↔	DDR8, DQ75, R	53	P032
2122,24,26	↔	DDR8, DQ76, R	55	P033
2122,24,26	↔	DDR8, DQ77, R	57	P034
2122,24,26	↔	DDR8, DQ78, R	60	P035
2122,24,26	↔	DDR8, DQ79, R	56	P054
2122,24,26	↔	DDR8, DQ80, R	146	P0514
2122,24,26	↔	DDR8, DQ81, R	146	P036
2122,24,26	↔	DDR8, DQ82, R	147	P037
2122,24,26	↔	DDR8, DQ83, R	150	P038
2122,24,26	↔	DDR8, DQ84, R	151	P039
2122,24,26	↔	DDR8, DQ85, R	61	P040
2122,24,26	↔	DDR8, DQ86, R	64	P041
2122,24,26	↔	DDR8, DQ87, R	68	P042
2122,24,26	↔	DDR8, DQ88, R	69	P043
2122,24,26	↔	DDR8, DQ89, R	67	P055
2122,24,26	↔	DDR8, DQ90, R	159	P0514
2122,24,26	↔	DDR8, DQ91, R	153	P044
2122,24,26	↔	DDR8, DQ92, R	155	P045
2122,24,26	↔	DDR8, DQ93, R	161	P046
2122,24,26	↔	DDR8, DQ94, R	162	P047
2122,24,26	↔	DDR8, DQ95, R	172	P048
2122,24,26	↔	DDR8, DQ96, R	73	P049
2122,24,26	↔	DDR8, DQ97, R	74	P050
2122,24,26	↔	DDR8, DQ98, R	80	P051
2122,24,26	↔	DDR8, DQ99, R	78	P052
2122,24,26	↔	DDR8, DQ100, R	165	P053
2122,24,26	↔	DDR8, DQ101, R	166	P054
2122,24,26	↔	DDR8, DQ102, R	171	P055
2122,24,26	↔	DDR8, DQ103, R	83	P056
2122,24,26	↔	DDR8, DQ104, R	84	P057
2122,24,26	↔	DDR8, DQ105, R	87	P058
2122,24,26	↔	DDR8, DQ106, R	88	P059
2122,24,26	↔	DDR8, DQ107, R	86	P057
2122,24,26	↔	DDR8, DQ108, R	177	P058
2122,24,26	↔	DDR8, DQ109, R	174	P059
2122,24,26	↔	DDR8, DQ110, R	175	P060
2122,24,26	↔	DDR8, DQ111, R	178	P061
2122,24,26	↔	DDR8, DQ112, R	179	P062
2122,24,26	↔	DDR8, DQ113, R	144	P063
2122,24,26	↔	DDR8, DQ114, R	44	P064
2122,24,26	↔	DDR8, DQ115, R	45	P065
2122,24,26	↔	DDR8, DQ116, R	46	P066
2122,24,26	↔	DDR8, DQ117, R	49	P067
2122,24,26	↔	DDR8, DQ118, R	51	P068
2122,24,26	↔	DDR8, DQ119, R	47	P069
2122,24,26	↔	DDR8, DQ120, R	140	P070
2122,24,26	↔	DDR8, DQ121, R	134	P071
2122,24,26	↔	DDR8, DQ122, R	135	P072
2122,24,26	↔	DDR8, DQ123, R	142	P073
2122,24,26	↔	DDR8, DQ124, R	144	P074
2122,24,26	↔	DDR8, DQ125, R	145	P075
2122,24,26	↔	DDR8, DQ126, R	146	P076
2122,24,26	↔	DDR8, DQ127, R	147	P077
2122,24,26	↔	DDR8, DQ128, R	148	P078
2122,24,26	↔	DDR8, DQ129, R	149	P079
2122,24,26	↔	DDR8, DQ130, R	150	P080
2122,24,26	↔	DDR8, DQ131, R	151	P081
2122,24,26	↔	DDR8, DQ132, R	152	P082
2122,24,26	↔	DDR8, DQ133, R	153	P083
2122,24,26	↔	DDR8, DQ134, R	154	P084
2122,24,26	↔	DDR8, DQ135, R	155	P085
2122,24,26	↔	DDR8, DQ136, R	156	P086
2122,24,26	↔	DDR8, DQ137, R	157	P087
2122,24,26	↔	DDR8, DQ138, R	158	P088
2122,24,26	↔	DDR8, DQ139, R	159	P089
2122,24,26	↔	DDR8, DQ140, R	160	P090
2122,24,26	↔	DDR8, DQ141, R	161	P091
2122,24,26	↔	DDR8, DQ142, R	162	P092
2122,24,26	↔	DDR8, DQ143, R	163	P093
2122,24,26	↔	DDR8, DQ144, R	164	P094
2122,24,26	↔	DDR8, DQ145, R	165	P095
2122,24,26	↔	DDR8, DQ146, R	166	P096
2122,24,26	↔	DDR8, DQ147, R	167	P097
2122,24,26	↔	DDR8, DQ148, R	168	P098
2122,24,26	↔	DDR8, DQ149, R	169	P099
2122,24,26	↔	DDR8, DQ150, R	170	P100
2122,24,26	↔	DDR8, DQ151, R	171	P101
2122,24,26	↔	DDR8, DQ152, R	172	P102
2122,24,26	↔	DDR8, DQ153, R	173	P103
2122,24,26	↔	DDR8, DQ154, R	174	P104
2122,24,26	↔	DDR8, DQ155, R	175	P105
2122,24,26	↔	DDR8, DQ156, R	176	P106
2122,24,26	↔	DDR8, DQ157, R	177	P107
2122,24,26	↔	DDR8, DQ158, R	178	P108
2122,24,26	↔	DDR8, DQ159, R	179	P109
2122,24,26	↔	DDR8, DQ160, R	180	P110
2122,24,26	↔	DDR8, DQ161, R	181	P111
2122,24,26	↔	DDR8, DQ162, R	182	P112
2122,24,26	↔	DDR8, DQ163, R	183	P113
2122,24,26	↔	DDR8, DQ164, R	184	P114
2122,24,26	↔	DDR8, DQ165, R	185	P115
2122,24,26	↔	DDR8, DQ166, R	186	P116
2122,24,26	↔	DDR8, DQ167, R	187	P117
2122,24,26	↔	DDR8, DQ168, R	188	P118
2122,24,26	↔	DDR8, DQ169, R	189	P119
2122,24,26	↔	DDR8, DQ170, R	190	P120
2122,24,26	↔	DDR8, DQ171, R	191	P121
2122,24,26	↔	DDR8, DQ172, R	192	P122
2122,24,26	↔	DDR8, DQ173, R	193	P123
2122,24,26	↔	DDR8, DQ174, R	194	P124
2122,24,26	↔	DDR8, DQ175, R	195	P125
2122,24,26	↔	DDR8, DQ176, R	196	P126
2122,24,26	↔	DDR8, DQ177, R	197	P127
2122,24,26	↔	DDR8, DQ178, R	198	P128
2122,24,26	↔	DDR8, DQ179, R	199	P129
2122,24,26	↔	DDR8, DQ180, R	200	P130
2122,24,26	↔	DDR8, DQ181, R	201	P131
2122,24,26	↔	DDR8, DQ182, R	202	P132
2122,24,26	↔	DDR8, DQ183, R	203	P133
2122,24,26	↔	DDR8, DQ184, R	204	P134
2122,24,26	↔	DDR8, DQ185, R	205	P135
2122,24,26	↔	DDR8, DQ186, R	206	P136
2122,24,26	↔	DDR8, DQ187, R	207	P137
2122,24,26	↔	DDR8, DQ188, R	208	P138
2122,24,26	↔	DDR8, DQ189, R	209	P139
2122,24,26	↔	DDR8, DQ190, R	210	P140
2122,24,26	↔	DDR8, DQ1		



16-19,22,24,62

VREF DDR DIMM

C1156  
0.1UF

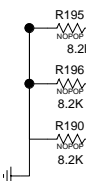
VDD ID  
16-19,22,24,60

21x2426 <-> DDRB D00 R	2	D00
21x2426 <-> DDRB D01 R	4	D01
21x2426 <-> DDRB D02 R	6	D02
21x2426 <-> DDRB D03 R	8	D03
21x2426 <-> DDRB D050 R	5	D050
21x2426 <-> DDRB D059 R	97	D059
21x2426 <-> DDRB D04 R	94	D04
21x2426 <-> DDRB D05 R	86	D05
21x2426 <-> DDRB D06 R	98	D06
21x2426 <-> DDRB D07 R	99	D07
21x2426 <-> DDRB D08 R	12	D08
21x2426 <-> DDRB D09 R	13	D09
21x2426 <-> DDRB D010 R	19	D010
21x2426 <-> DDRB D011 R	20	D011
21x2426 <-> DDRB D081 R	14	D081
21x2426 <-> DDRB D0510 R	107	D0510
21x2426 <-> DDRB D012 R	105	D012
21x2426 <-> DDRB D013 R	106	D013
21x2426 <-> DDRB D014 R	109	D014
21x2426 <-> DDRB D015 R	110	D015
21x2426 <-> DDRB D016 R	23	D016
21x2426 <-> DDRB D017 R	24	D017
21x2426 <-> DDRB D018 R	26	D018
21x2426 <-> DDRB D019 R	31	D019
21x2426 <-> DDRB D052 R	25	D052
21x2426 <-> DDRB D0811 R	119	D0811
21x2426 <-> DDRB D020 R	117	D020
21x2426 <-> DDRB D021 R	121	D021
21x2426 <-> DDRB D022 R	123	D022
21x2426 <-> DDRB D023 R	123	D023
21x2426 <-> DDRB D024 R	33	D024
21x2426 <-> DDRB D025 R	35	D025
21x2426 <-> DDRB D026 R	39	D026
21x2426 <-> DDRB D027 R	40	D027
21x2426 <-> DDRB D053 R	36	D053
21x2426 <-> DDRB D0512 R	129	D0512
21x2426 <-> DDRB D028 R	126	D028
21x2426 <-> DDRB D029 R	127	D029
21x2426 <-> DDRB D030 R	131	D030
21x2426 <-> DDRB D031 R	133	D031
21x2426 <-> DDRB D032 R	53	D032
21x2426 <-> DDRB D033 R	55	D033
21x2426 <-> DDRB D034 R	57	D034
21x2426 <-> DDRB D035 R	60	D035
21x2426 <-> DDRB D054 R	56	D054
21x2426 <-> DDRB D0813 R	149	D0813
21x2426 <-> DDRB D036 R	146	D036
21x2426 <-> DDRB D037 R	147	D037
21x2426 <-> DDRB D038 R	150	D038
21x2426 <-> DDRB D039 R	151	D039
21x2426 <-> DDRB D040 R	61	D040
21x2426 <-> DDRB D041 R	64	D041
21x2426 <-> DDRB D042 R	68	D042
21x2426 <-> DDRB D043 R	69	D043
21x2426 <-> DDRB D055 R	67	D055
21x2426 <-> DDRB D0514 R	159	D0514
21x2426 <-> DDRB D044 R	153	D044
21x2426 <-> DDRB D045 R	155	D045
21x2426 <-> DDRB D046 R	161	D046
21x2426 <-> DDRB D047 R	162	D047
21x2426 <-> DDRB D048 R	72	D048
21x2426 <-> DDRB D049 R	73	D049
21x2426 <-> DDRB D050 R	79	D050
21x2426 <-> DDRB D051 R	80	D051
21x2426 <-> DDRB D056 R	78	D056
21x2426 <-> DDRB D0815 R	169	D0815
21x2426 <-> DDRB D053 R	165	D053
21x2426 <-> DDRB D053 R	166	D053
21x2426 <-> DDRB D054 R	170	D054
21x2426 <-> DDRB D055 R	171	D055
21x2426 <-> DDRB D056 R	83	D056
21x2426 <-> DDRB D057 R	84	D057
21x2426 <-> DDRB D058 R	87	D058
21x2426 <-> DDRB D059 R	88	D059
21x2426 <-> DDRB D057 R	86	D057
21x2426 <-> DDRB D0516 R	177	D0516
21x2426 <-> DDRB D060 R	174	D060
21x2426 <-> DDRB D061 R	175	D061
21x2426 <-> DDRB D062 R	178	D062
21x2426 <-> DDRB D063 R	179	D063
21x2426 <-> DDRB D60 R	44	D60
21x2426 <-> DDRB D61 R	46	D61
21x2426 <-> DDRB D62 R	49	D62
21x2426 <-> DDRB D63 R	51	D63
21x2426 <-> DDRB D058 R	47	D058
21x2426 <-> DDRB D0517 R	140	D0517
21x2426 <-> DDRB D64 R	134	D64
21x2426 <-> DDRB D65 R	135	D65
21x2426 <-> DDRB D66 R	142	D66
21x2426 <-> DDRB D67 R	144	D67

# DDR DIMM

DIMM B-4

VREF	50	<13,22,24,26
VSS1	3	<13,22,24,26
VSS2	11	<13,22,24,26
VSS3	18	<13,22,24,26
VSS4	26	<13,22,24,26
VSS5	34	<13,22,24,26
VSS6	42	<13,22,24,26
VSS7	58	<13,22,24,26
VSS8	66	<13,22,24,26
VSS9	74	<13,22,24,26
VSS10	81	<13,22,24,26
VSS11	89	<13,22,24,26
VSS12	176	<13,22,24,26
VSS13	160	<13,22,24,26
VSS14	152	<13,22,24,26
VSS15	145	<13,22,24,26
VSS16	139	<13,22,24,26
VSS17	132	<13,22,24,26
VSS18	124	<13,22,24,26
VSS19	116	<13,22,24,26
VSS20	110	<13,22,24,26
VSS21	93	<13,22,24,26
VSS22	82	<13,22,24,26
VDD10	7	<13,22,24,26
VDD1	38	<13,22,24,26
VDD2	46	<13,22,24,26
VDD3	70	<13,22,24,26
VDD4	85	<13,22,24,26
VDD5	168	<13,22,24,26
VDD6	148	<13,22,24,26
VDD7	120	<13,22,24,26
VDD8	108	<13,22,24,26
VDD9	15	<13,22,24,26
VDD10	22	<13,22,24,26
VDD11	30	<13,22,24,26
VDD12	54	<13,22,24,26
VDD13	62	<13,22,24,26
VDD14	77	<13,22,24,26
VDD15	180	<13,22,24,26
VDD16	172	<13,22,24,26
VDD17	164	<13,22,24,26
VDD18	156	<13,22,24,26
VDD19	143	<13,22,24,26
VDD20	136	<13,22,24,26
VDD21	128	<13,22,24,26
VDD22	104	<13,22,24,26
VDD23	96	<13,22,24,26
VDD24	48	<13,22,24,26
VDD25	43	<13,22,24,26
VDD26	41	<13,22,24,26
VDD27	130	<13,22,24,26
VDD28	37	<13,22,24,26
VDD29	32	<13,22,24,26
VDD30	125	<13,22,24,26
VDD31	29	<13,22,24,26
VDD32	27	<13,22,24,26
VDD33	141	<13,22,24,26
VDD34	119	<13,20,22,24
VDD35	115	<13,22,24,26
VDD36	103	<13,22,24,26
VDD37	83	<13,22,24,26
VDD38	65	<13,22,24,26
VDD39	154	<13,20,22,24
VDD40	9	<13,20,22,24
VDD41	90	<13,22,24,26
VDD42	173	<13,22,24,26
VDD43	102	<13,22,24,26
VDD44	101	<13,22,24,26
VDD45	71	<13,22,24,26
VDD46	163	<13,22,24,26
VDD47	167	<13,22,24,26
VDD48	10	<11,16-18,22,24,53
VDD49	16	<11,16-18,22,24,53
VDD50	17	<11,16-18,22,24,53
VDD51	75	<11,16-18,22,24,53
VDD52	76	<11,16-18,22,24,53
VDD53	21	<13,22,24,26
VDD54	111	<13,22,24,26
VDD55	59	<13,22,24,26
VDD56	52	<13,22,24,26
VDD57	113	<13,22,24,26
VDD58	137	<13,22,24,26
VDD59	139	<13,22,24,26
VDD60	91	<16-19,22,24,60,61
VDD61	92	<16-19,22,24,60,61
VDD62	181	<16-19,22,24,60,61
VDD63	182	<16-19,22,24,60,61
VDD64	183	<16-19,22,24,60,61
VDD65	157	<13,20
VDD66	159	<13,20







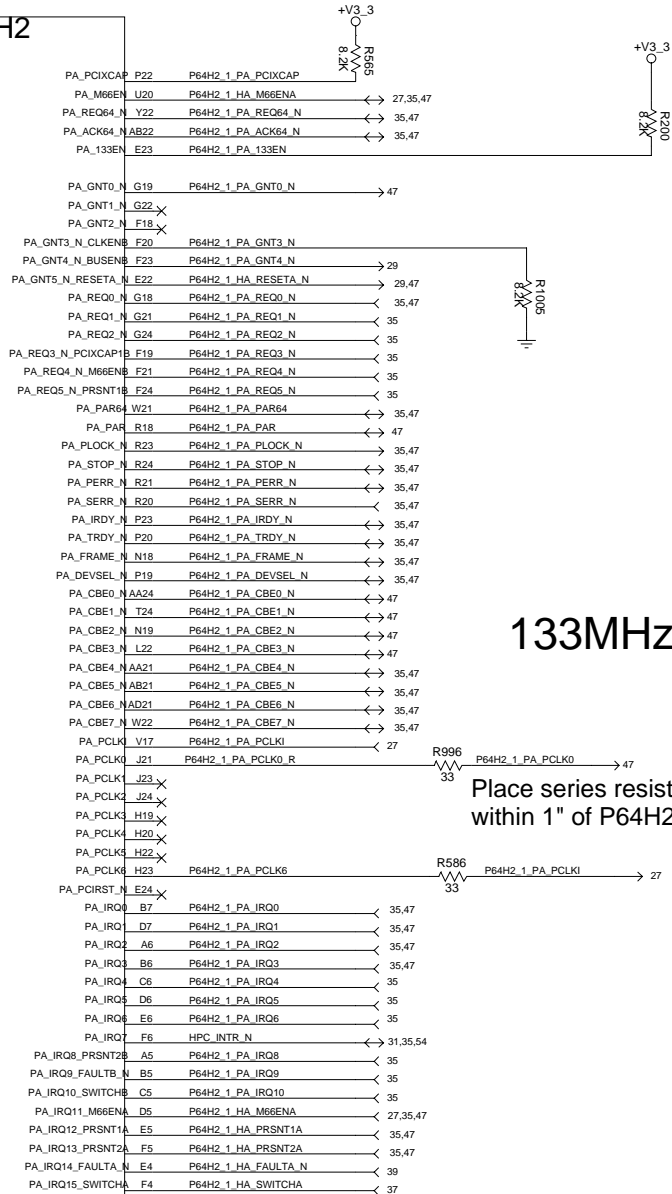
35,47 ← P64H2\_1\_PA\_AD[63:0]

P64H2_1_PA_AD0	AC22	PA_AD0
P64H2_1_PA_AD1	Y23	PA_AD1
P64H2_1_PA_AD2	Y23	PA_AD2
P64H2_1_PA_AD3	AA23	PA_AD3
P64H2_1_PA_AD4	AC23	PA_AD4
P64H2_1_PA_AD5	AD23	PA_AD5
P64H2_1_PA_AD6	V24	PA_AD6
P64H2_1_PA_AD7	W24	PA_AD7
P64H2_1_PA_AD8	AB24	PA_AD8
P64H2_1_PA_AD9	U19	PA_AD9
P64H2_1_PA_AD10	U22	PA_AD10
P64H2_1_PA_AD11	U23	PA_AD11
P64H2_1_PA_AD12	T18	PA_AD12
P64H2_1_PA_AD13	T19	PA_AD13
P64H2_1_PA_AD14	T21	PA_AD14
P64H2_1_PA_AD15	T22	PA_AD15
P64H2_1_PA_AD16	N21	PA_AD16
P64H2_1_PA_AD17	N22	PA_AD17
P64H2_1_PA_AD18	M18	PA_AD18
P64H2_1_PA_AD19	M20	PA_AD19
P64H2_1_PA_AD20	M21	PA_AD20
P64H2_1_PA_AD21	M23	PA_AD21
P64H2_1_PA_AD22	L19	PA_AD22
P64H2_1_PA_AD23	L20	PA_AD23
P64H2_1_PA_AD24	L23	PA_AD24
P64H2_1_PA_AD25	K18	PA_AD25
P64H2_1_PA_AD26	K19	PA_AD26
P64H2_1_PA_AD27	K21	PA_AD27
P64H2_1_PA_AD28	K22	PA_AD28
P64H2_1_PA_AD29	K24	PA_AD29
P64H2_1_PA_AD30	J18	PA_AD30
P64H2_1_PA_AD31	J20	PA_AD31
P64H2_1_PA_AD32	V14	PA_AD32
P64H2_1_PA_AD33	Y14	PA_AD33
P64H2_1_PA_AD34	AA14	PA_AD34
P64H2_1_PA_AD35	AC14	PA_AD35
P64H2_1_PA_AD36	AD14	PA_AD36
P64H2_1_PA_AD37	V15	PA_AD37
P64H2_1_PA_AD38	W15	PA_AD38
P64H2_1_PA_AD39	AA15	PA_AD39
P64H2_1_PA_AD40	AB15	PA_AD40
P64H2_1_PA_AD41	AD15	PA_AD41
P64H2_1_PA_AD42	W16	PA_AD42
P64H2_1_PA_AD43	Y16	PA_AD43
P64H2_1_PA_AD44	AB16	PA_AD44
P64H2_1_PA_AD45	AC16	PA_AD45
P64H2_1_PA_AD46	Y17	PA_AD46
P64H2_1_PA_AD47	AA17	PA_AD47
P64H2_1_PA_AD48	AC17	PA_AD48
P64H2_1_PA_AD49	AD17	PA_AD49
P64H2_1_PA_AD50	W18	PA_AD50
P64H2_1_PA_AD51	AA18	PA_AD51
P64H2_1_PA_AD52	AB18	PA_AD52
P64H2_1_PA_AD53	AD18	PA_AD53
P64H2_1_PA_AD54	W19	PA_AD54
P64H2_1_PA_AD55	Y19	PA_AD55
P64H2_1_PA_AD56	AB19	PA_AD56
P64H2_1_PA_AD57	AC19	PA_AD57
P64H2_1_PA_AD58	V20	PA_AD58
P64H2_1_PA_AD59	Y20	PA_AD59
P64H2_1_PA_AD60	AA20	PA_AD60
P64H2_1_PA_AD61	AC20	PA_AD61
P64H2_1_PA_AD62	AD20	PA_AD62
P64H2_1_PA_AD63	V21	PA_AD63

U14

P64H2

PCI\_X\_INTERFACE\_A



133MHz Slot 1

Place series resistors  
within 1" of P64H2

P64H2 #1

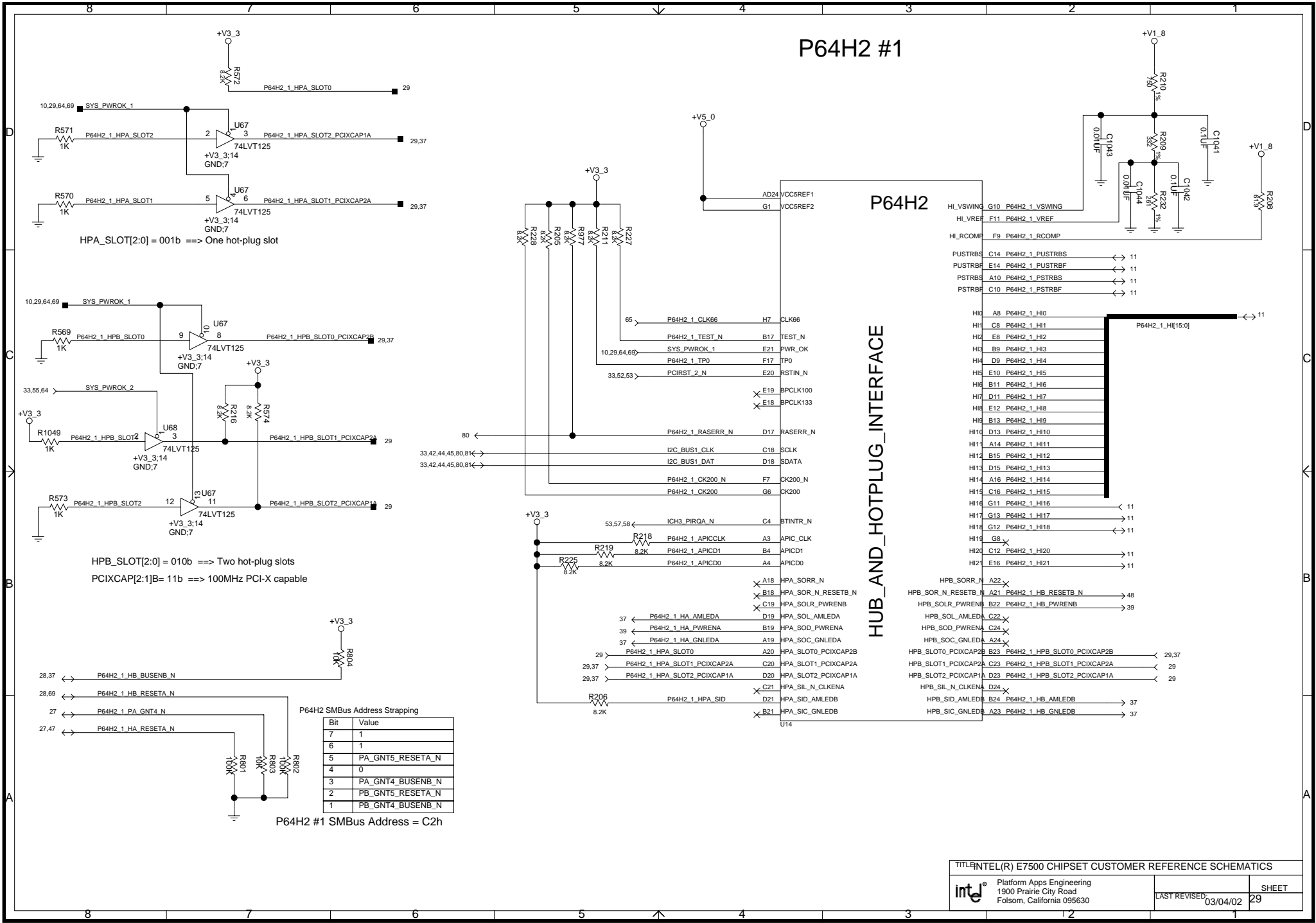


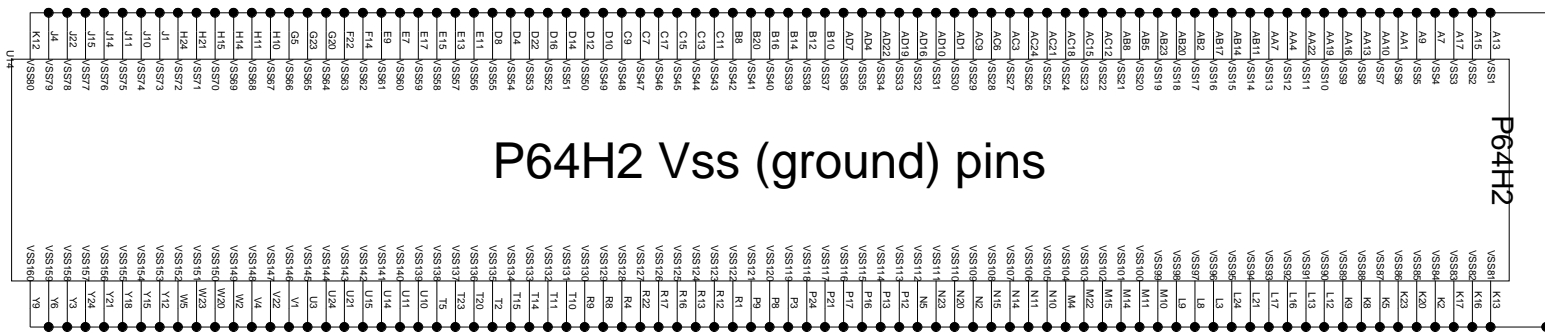
Place series resistors  
within 1" of P64H2

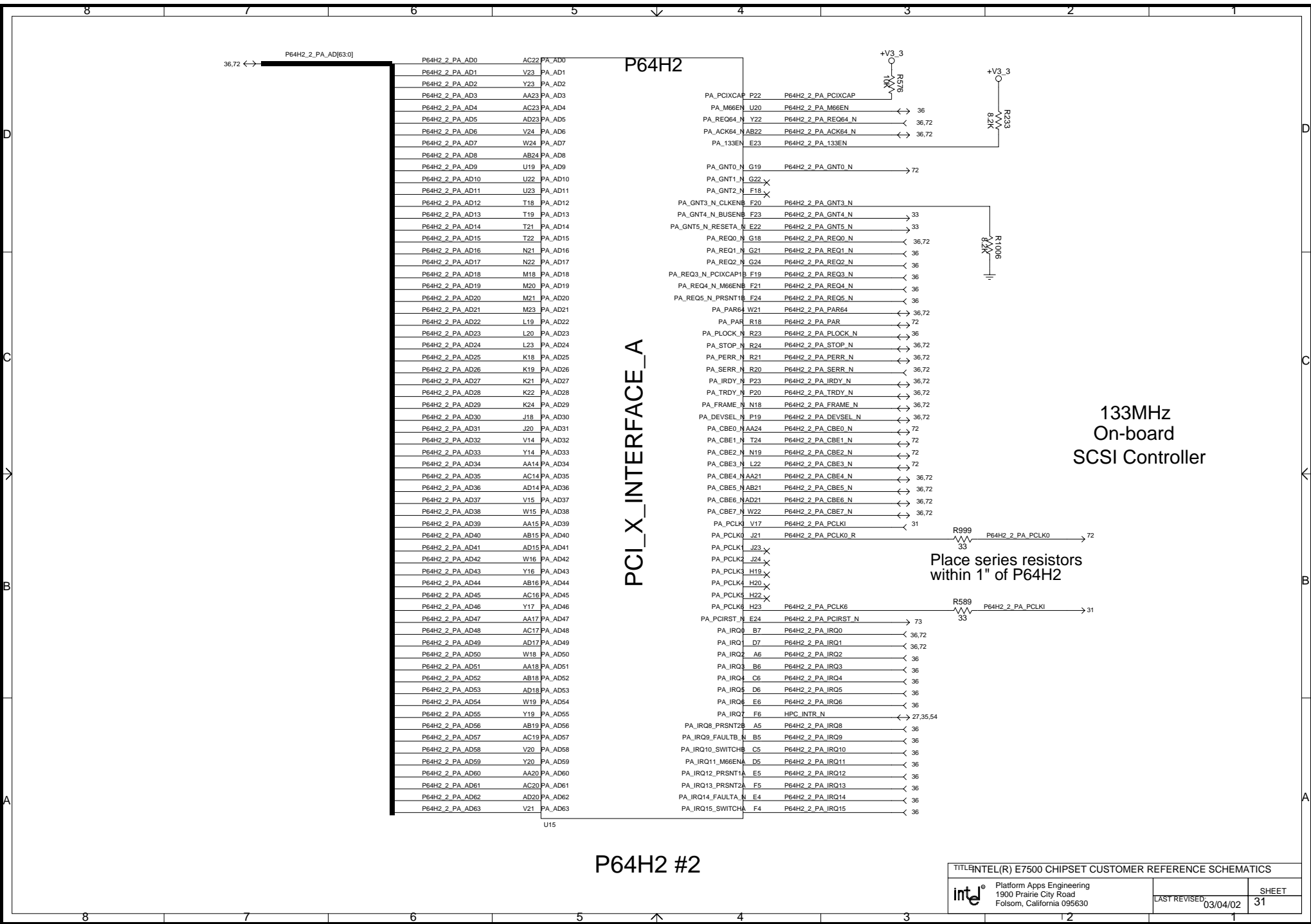
# P64H2 #1

## P64H2

### HUB\_AND\_HOTPLUG\_INTERFACE





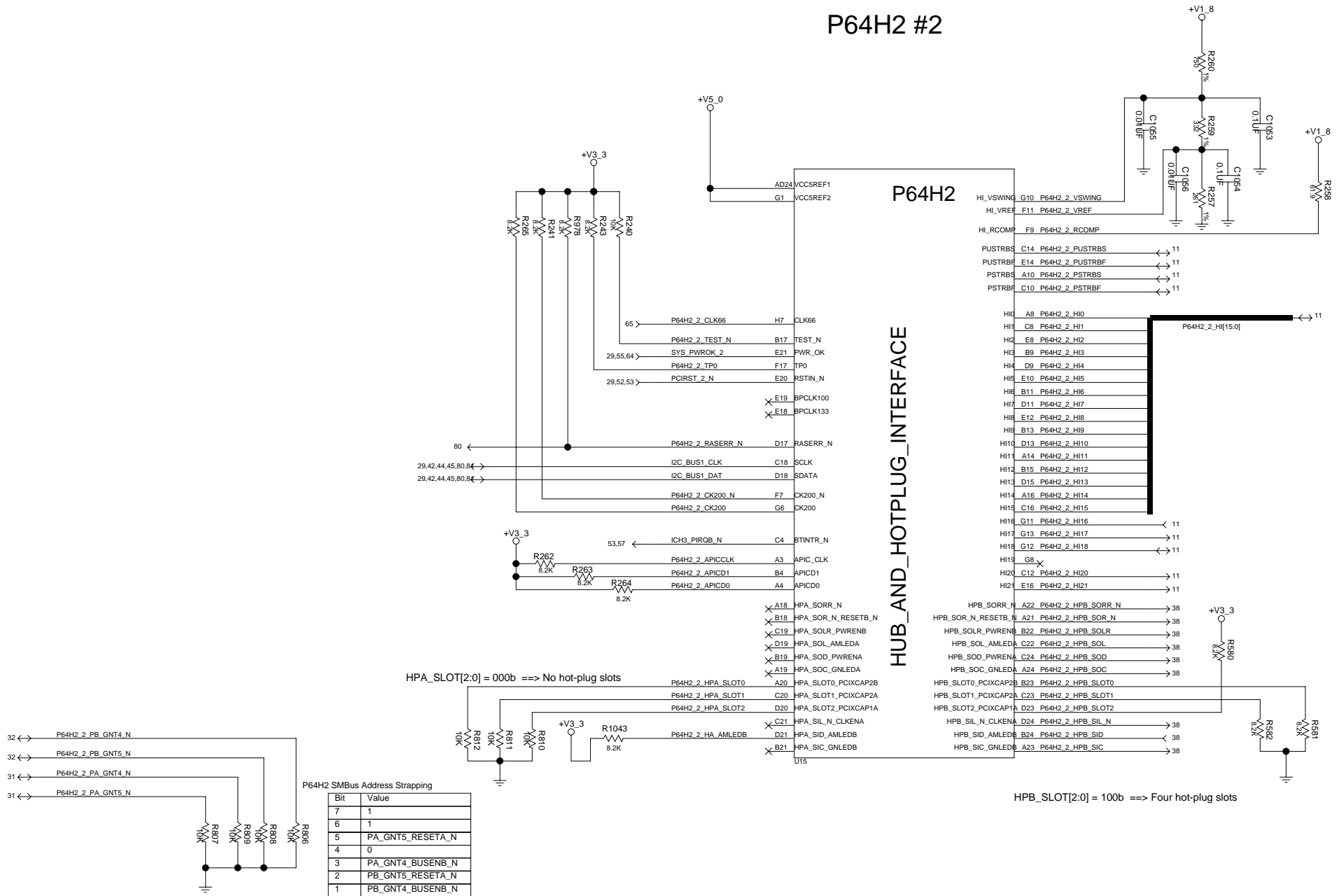


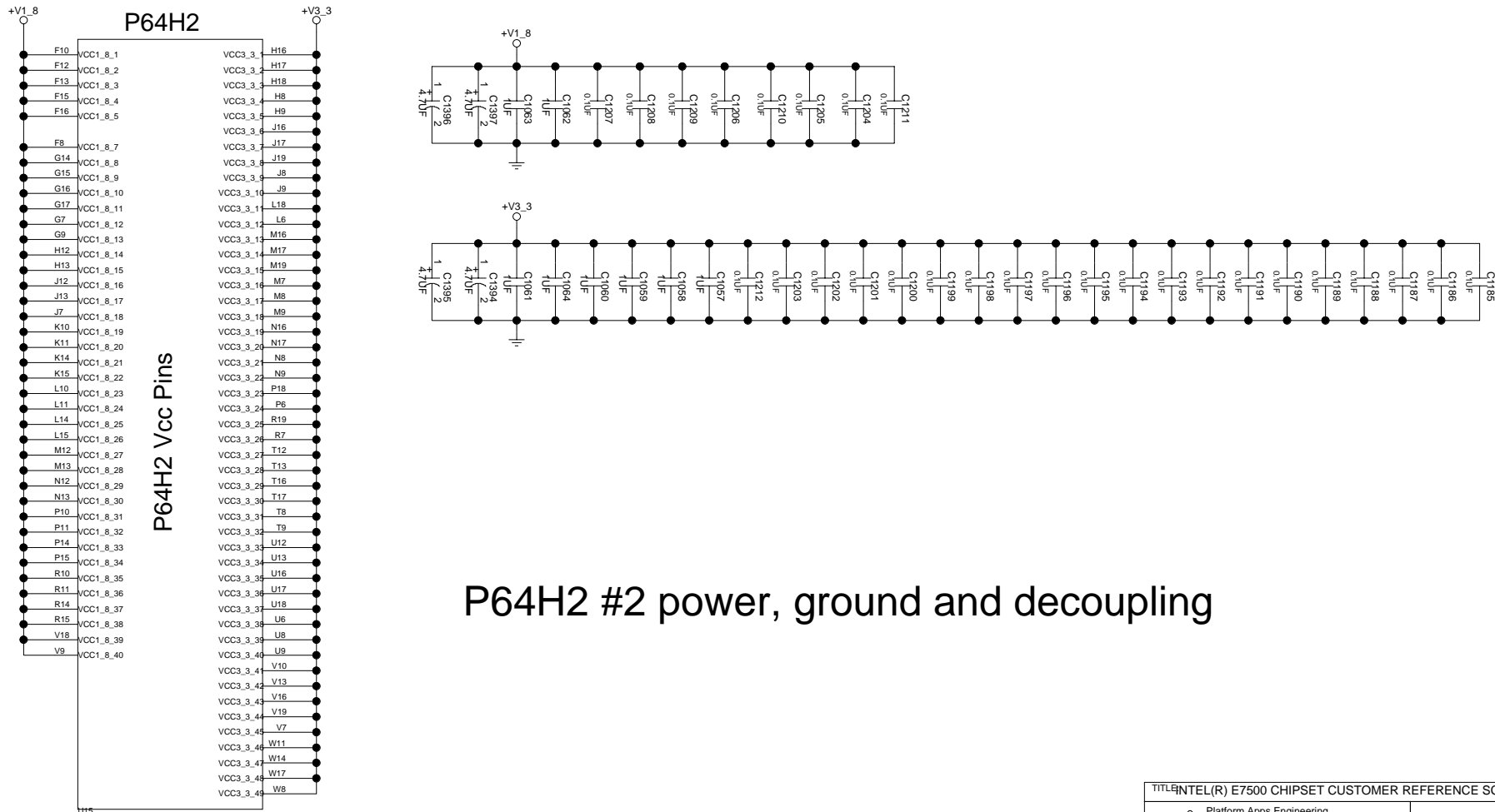
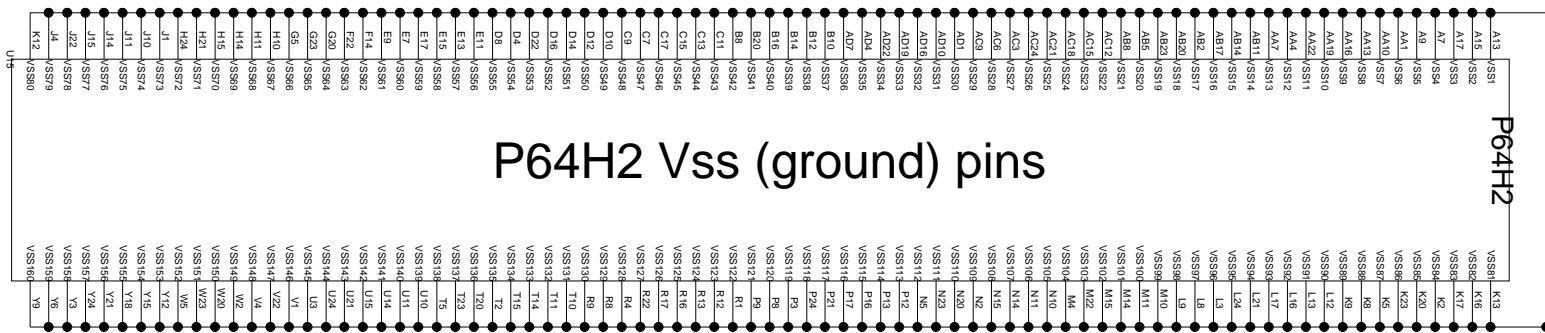


# P64H2 #2

## P64H2

### HUB\_AND\_HOTPLUG\_INTERFACE

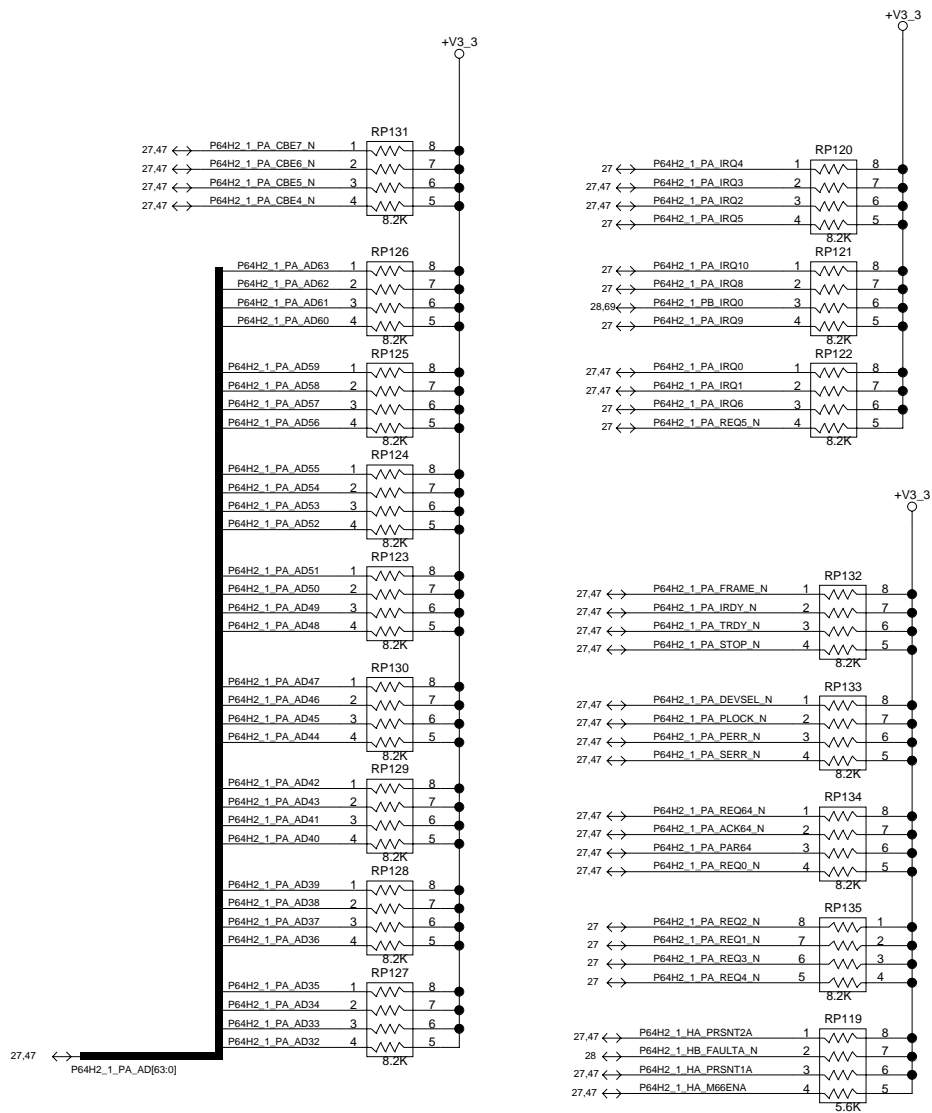




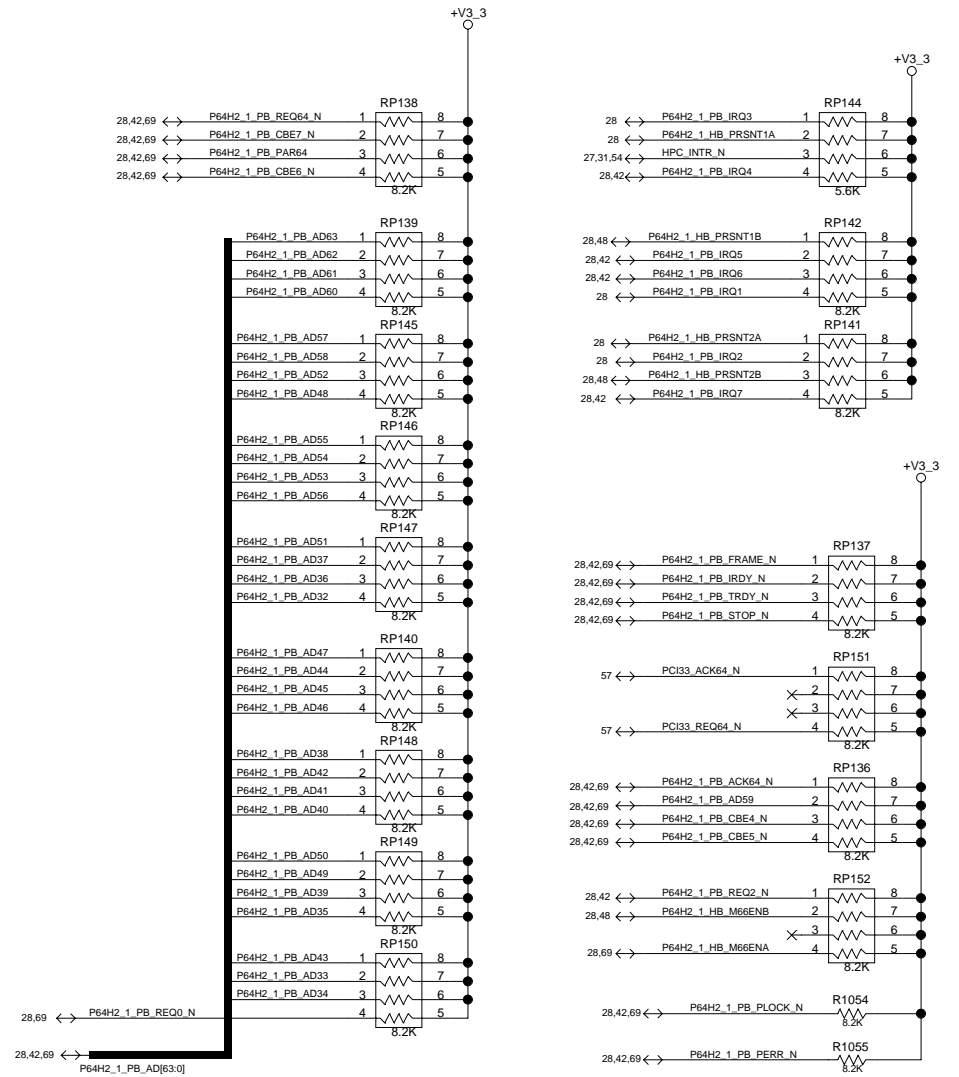
P64H2 #2 power, ground and decoupling



P64H2 #1 PCI Bus A pull-ups



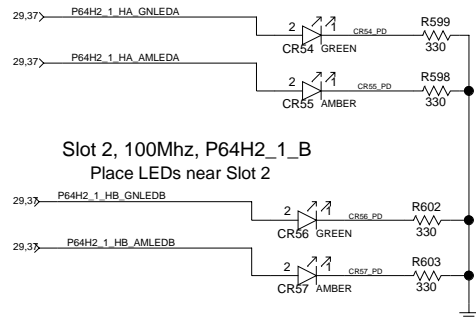
P64H2 #1 PCI Bus B pull-ups





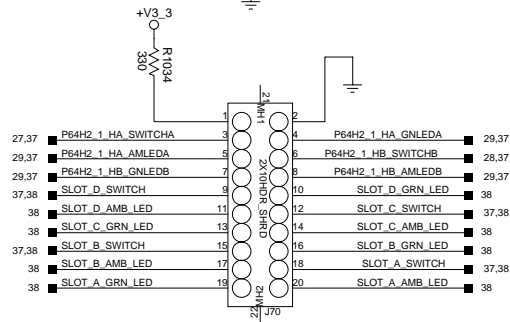
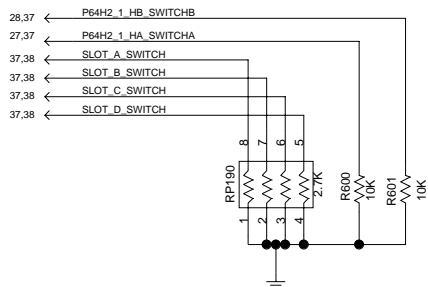
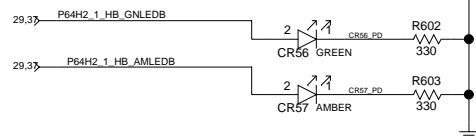
# Slot 1, 133Mhz, P64H2\_1\_A

Place LEDs near Slot 1

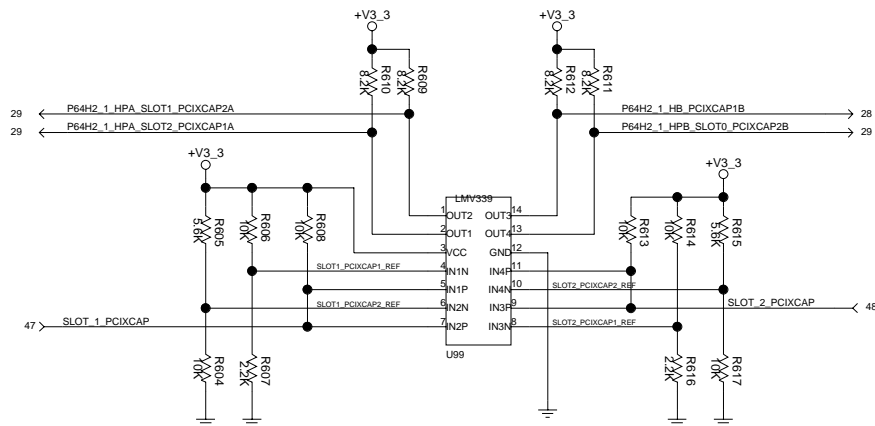
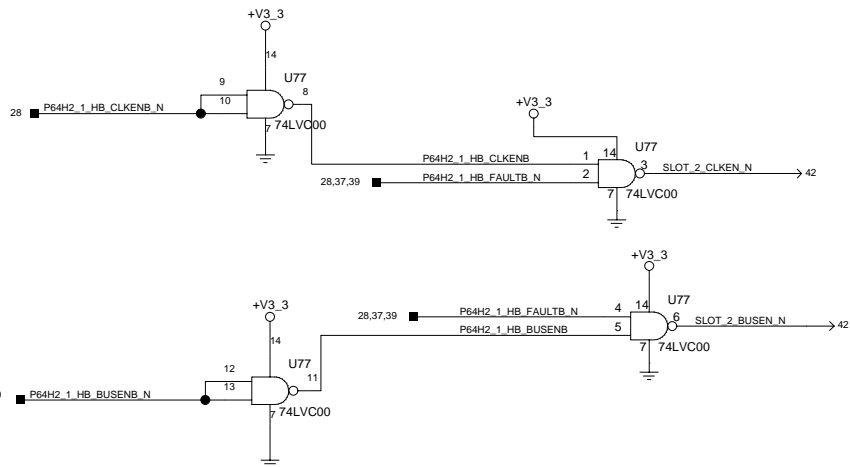


# Slot 2, 100Mhz, P64H2\_1\_B

Place LEDs near Slot 2



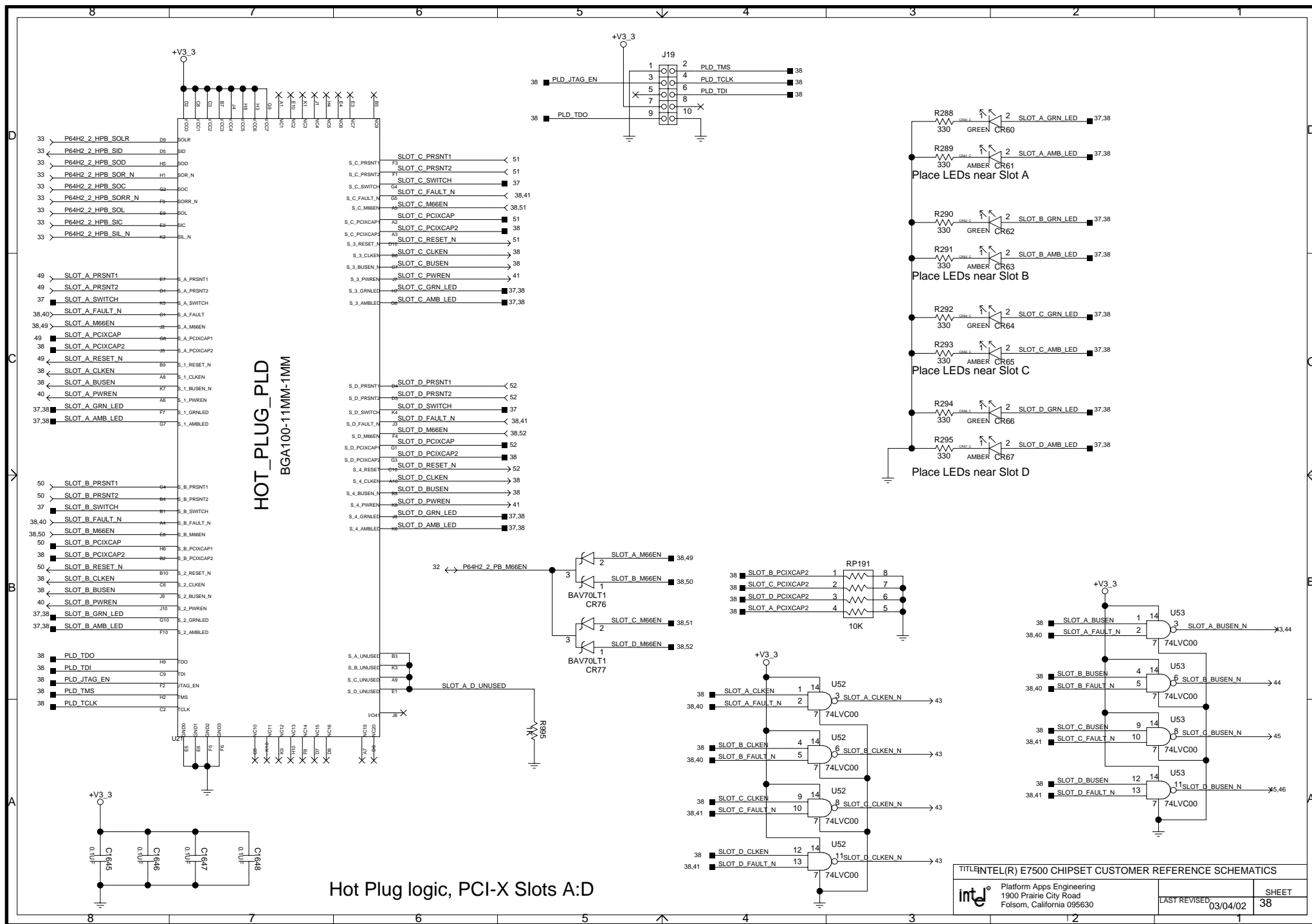
Chassis hot-plug switch  
board connector

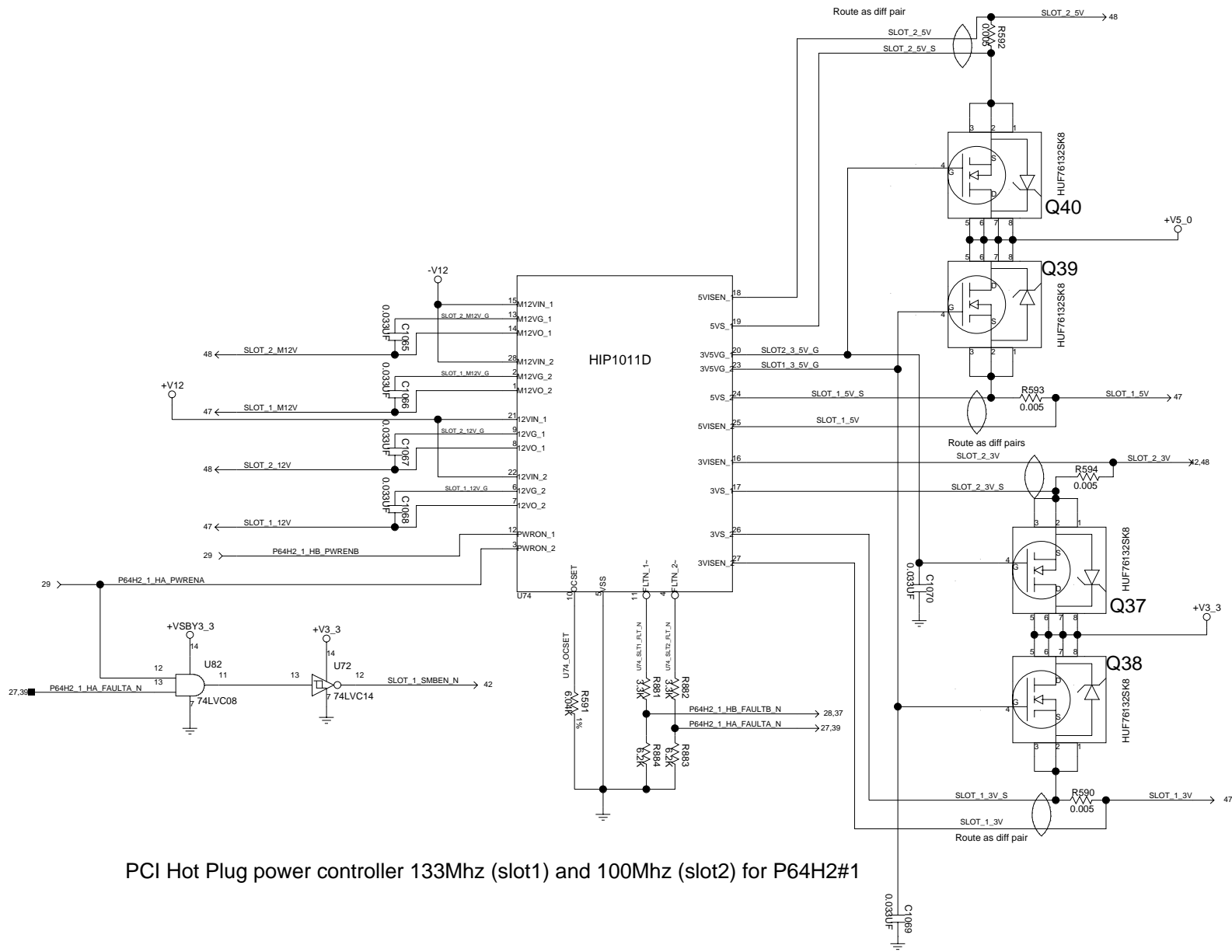


Slot 1, 133Mhz, P64H2\_1\_A & Slot 2, 100Mhz, P64H2\_1\_B

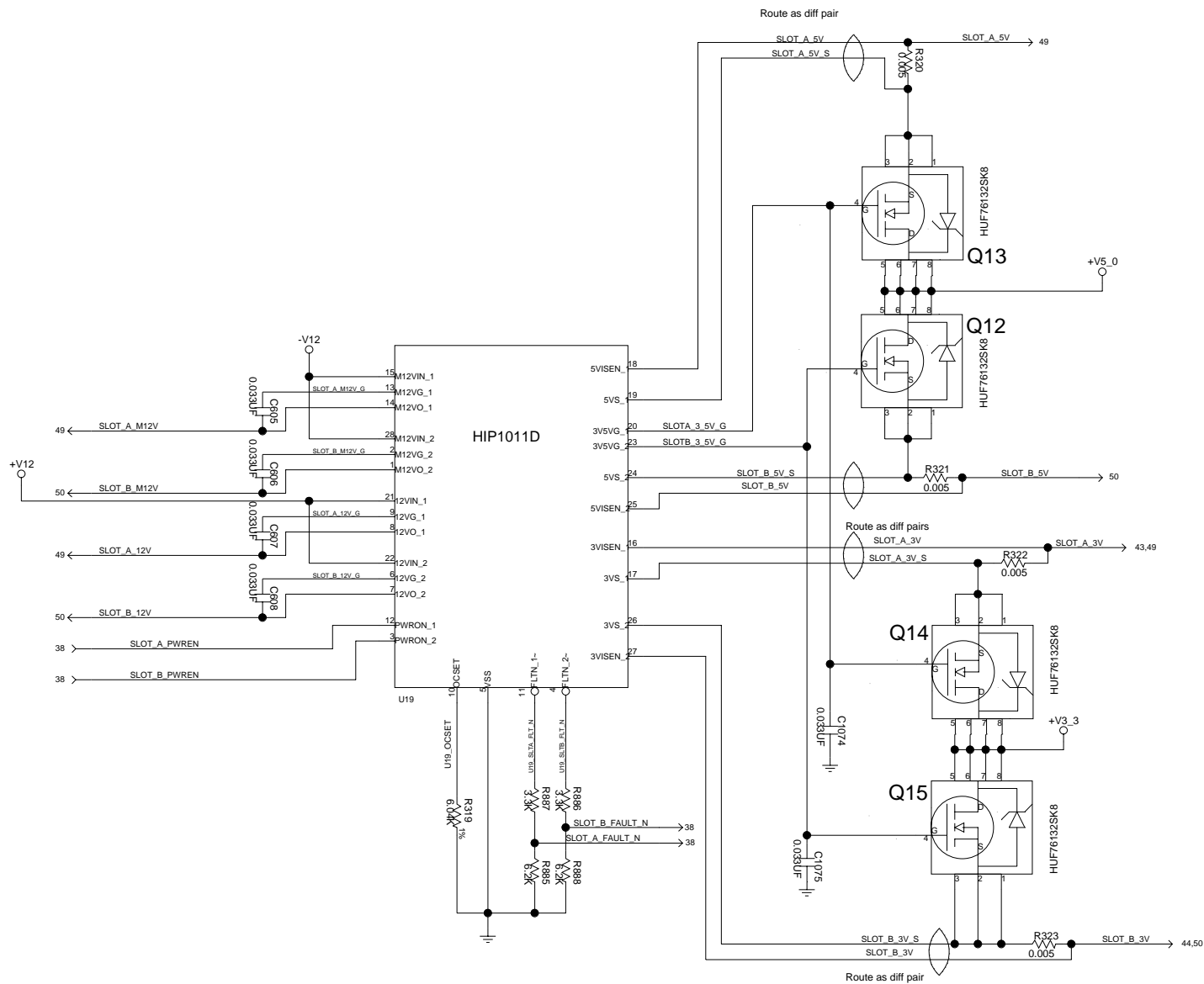
PCIXCAP Comparators, bus and clk enable gates

Hot Plug logic, PCI-X Slots 1,2



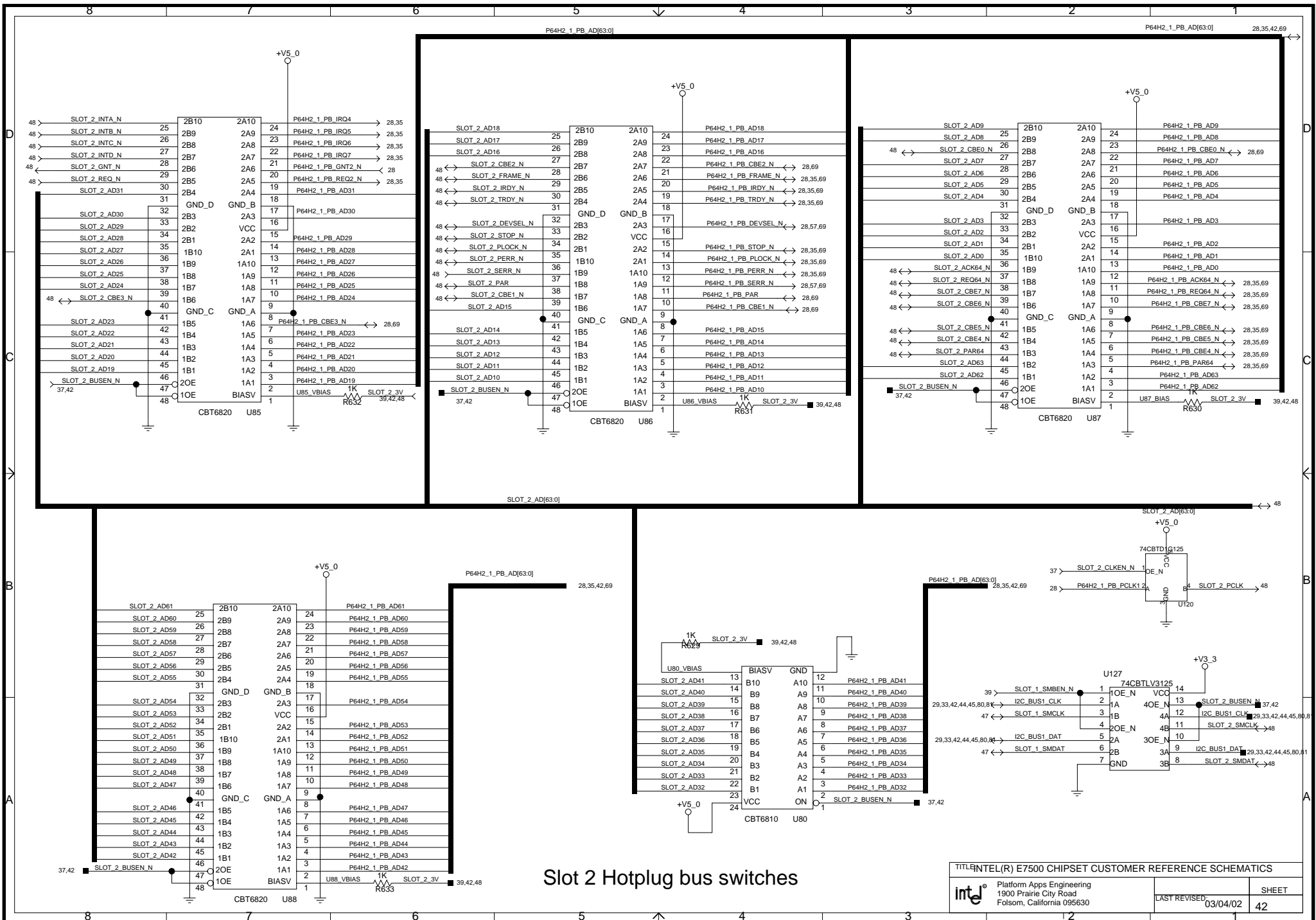


PCI Hot Plug power controller 133Mhz (slot1) and 100Mhz (slot2) for P64H2#1



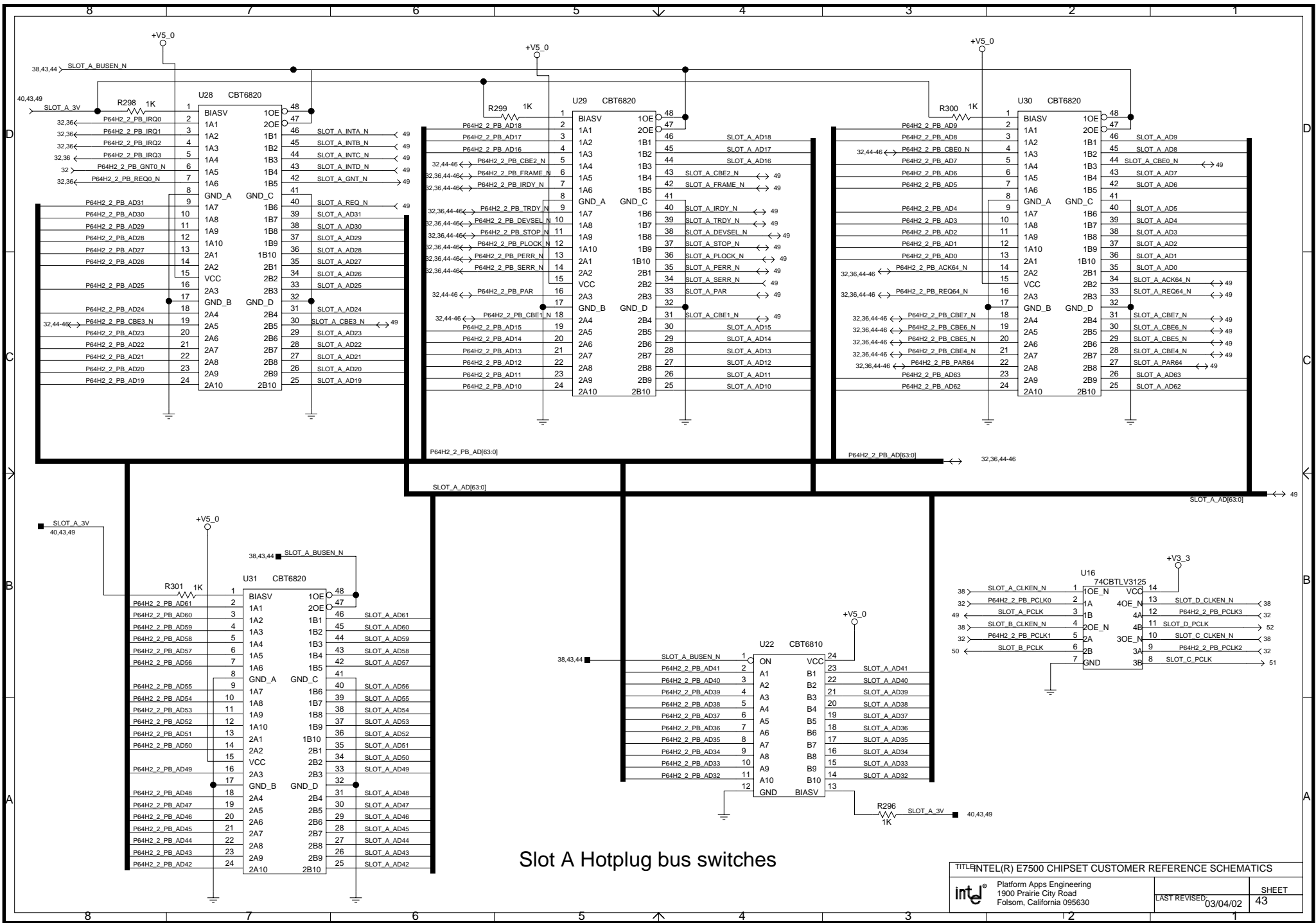
PCI Hot Plug power control. 66MHz Slots A and B

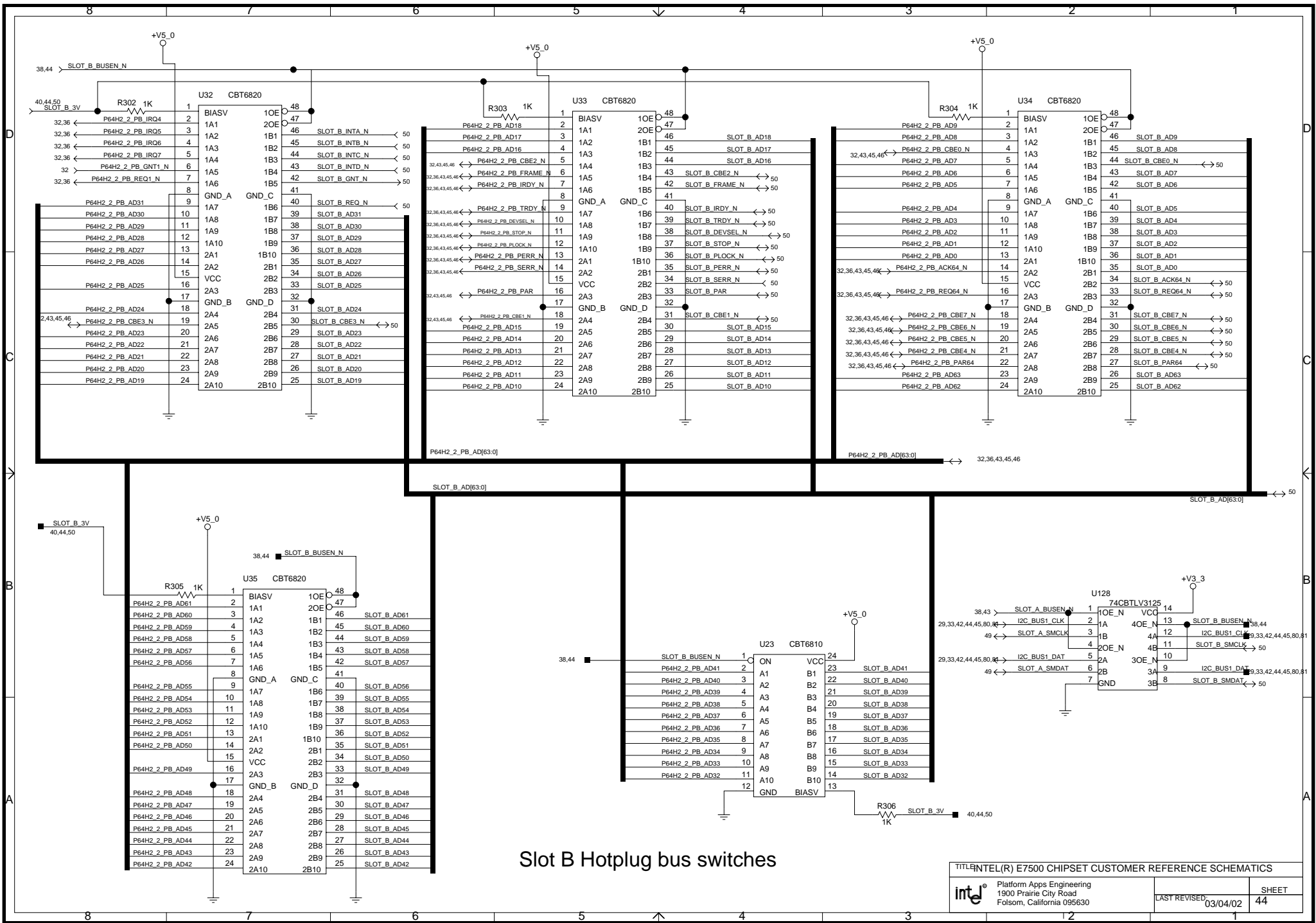




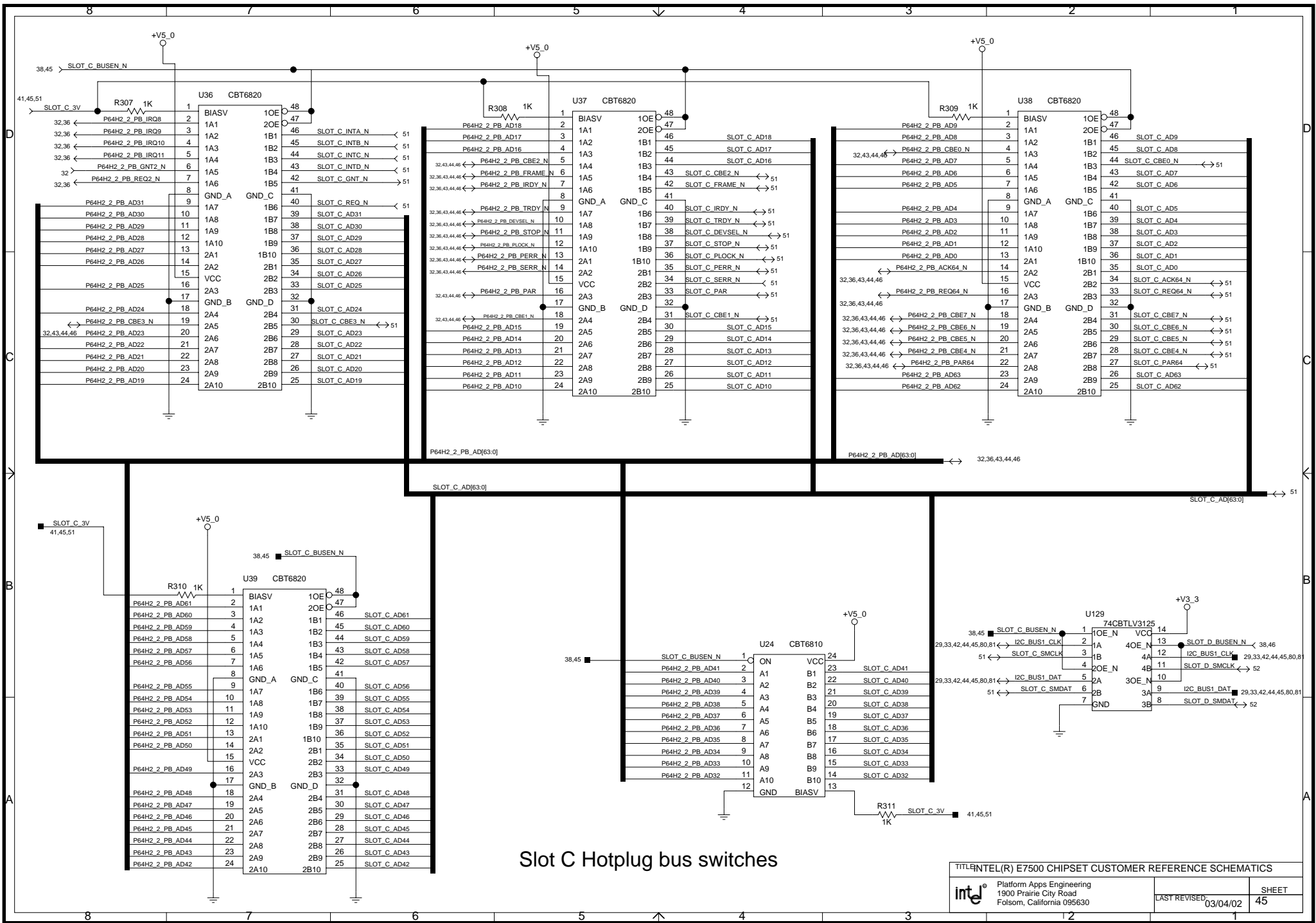
Slot 2 Hotplug bus switches







Slot B Hotplug bus switches

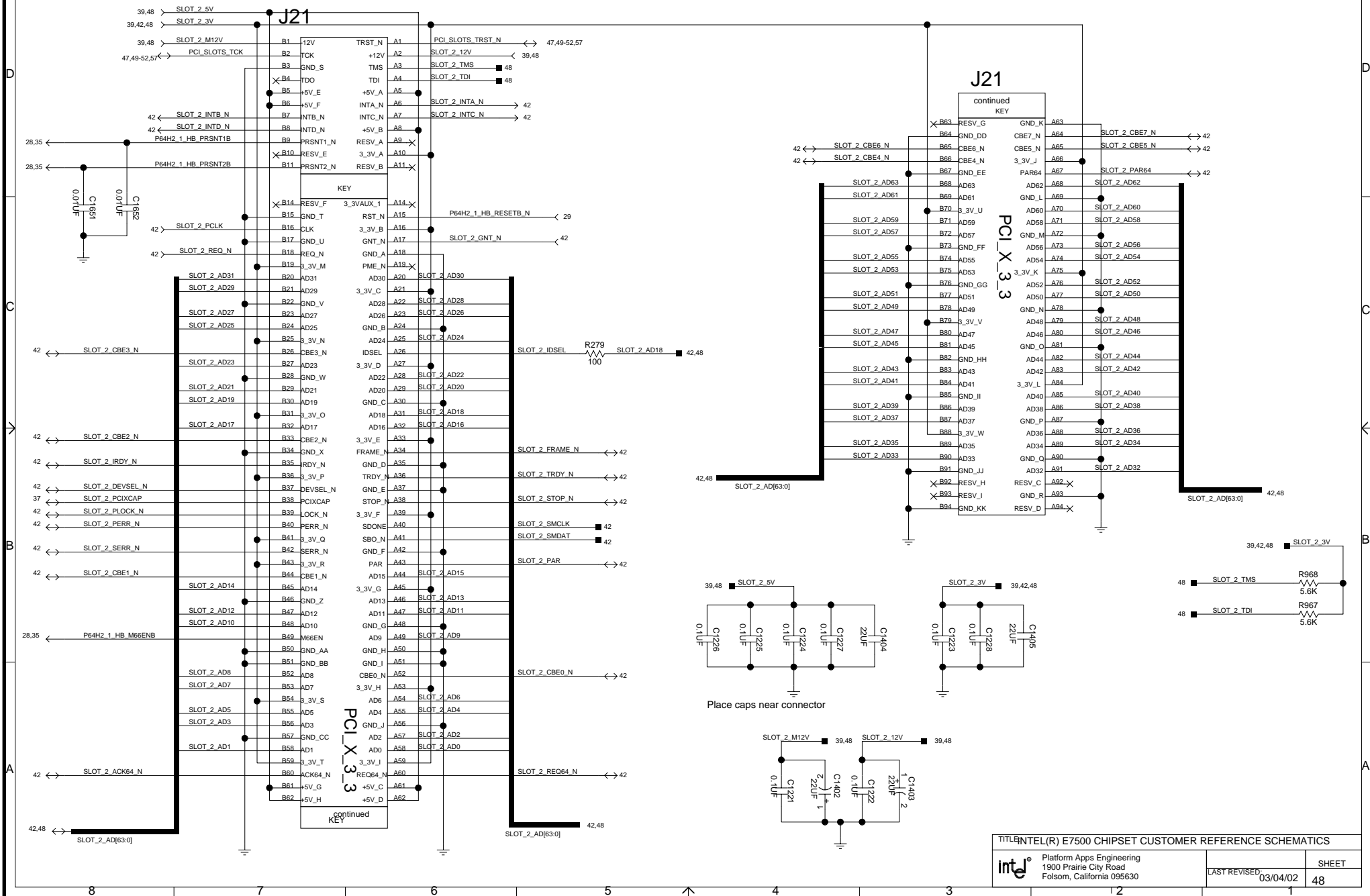


Slot C Hotplug bus switches

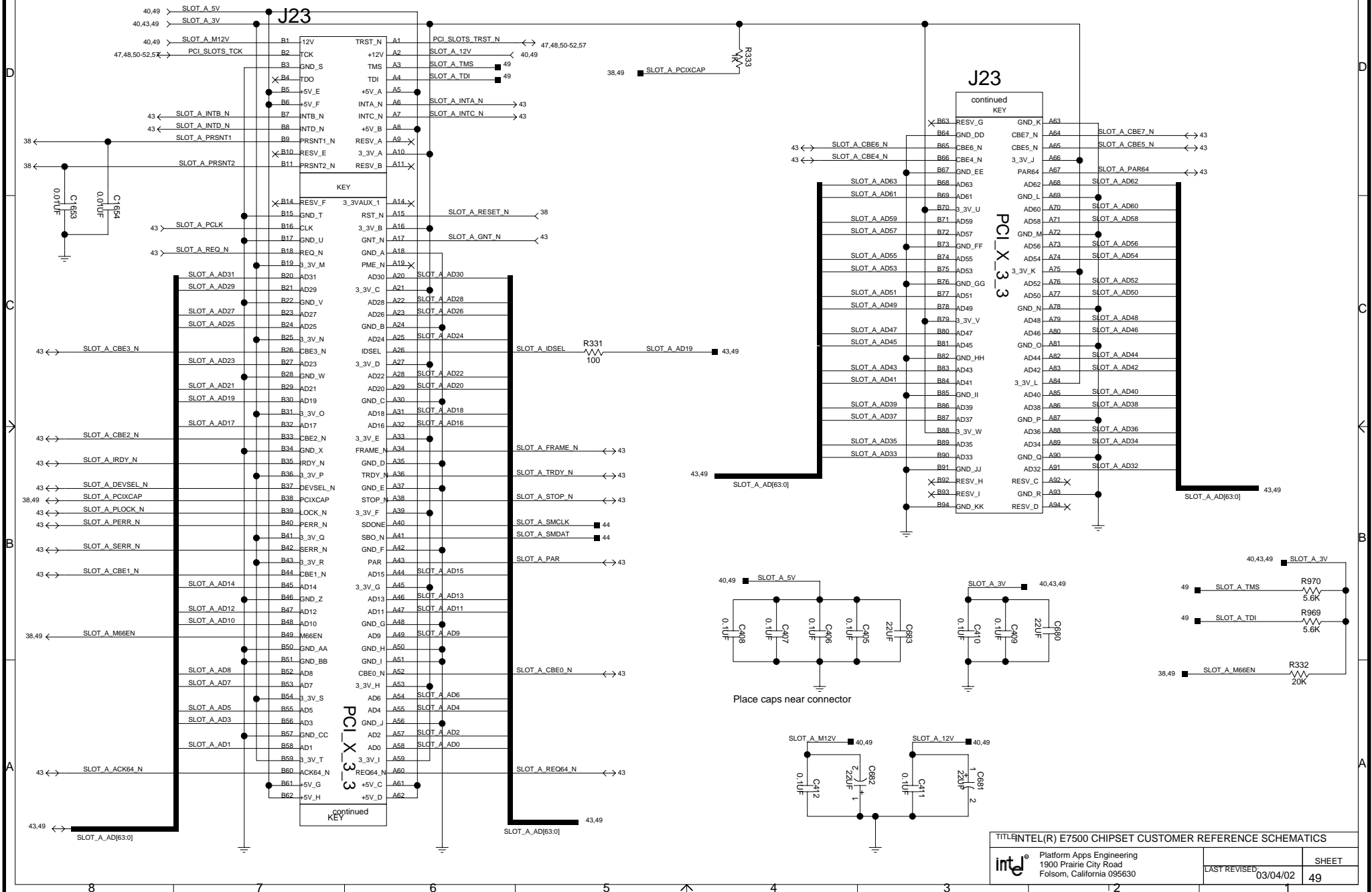


[illegible][illegible]

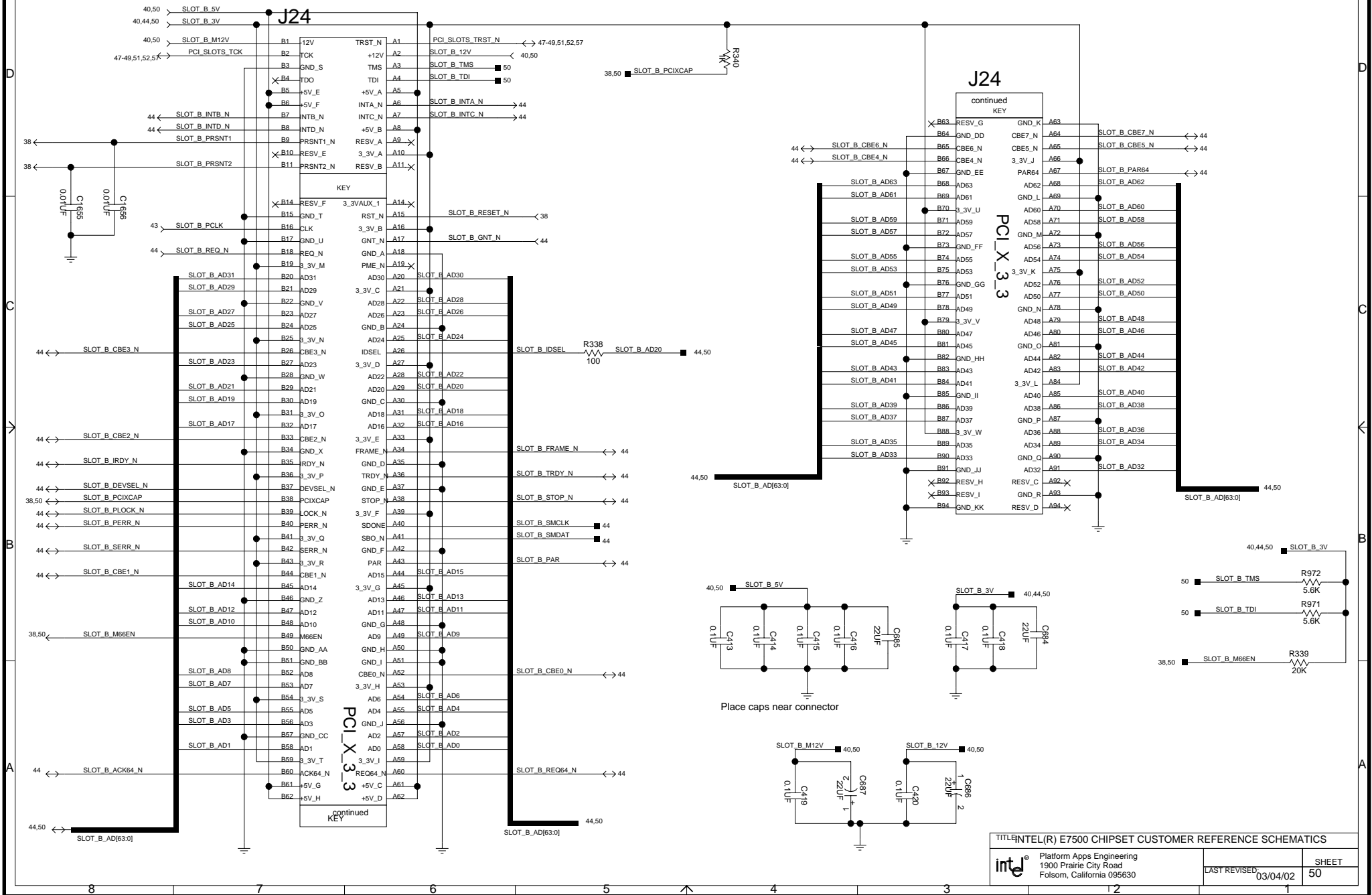
## PCI-X Slot 2 (P64H2 #1, PCI Bus B)



# PCI-X 66MHz SLOT A



# PCI-X 66MHz SLOT B





**PCI-X 66MHz SLOT C**

**J25**

**continued KEY**

**KEY**

**PCI\_X\_3\_3**

**continued KEY**

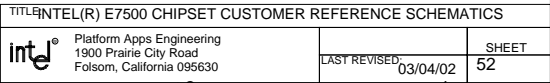
**Place caps near connector**

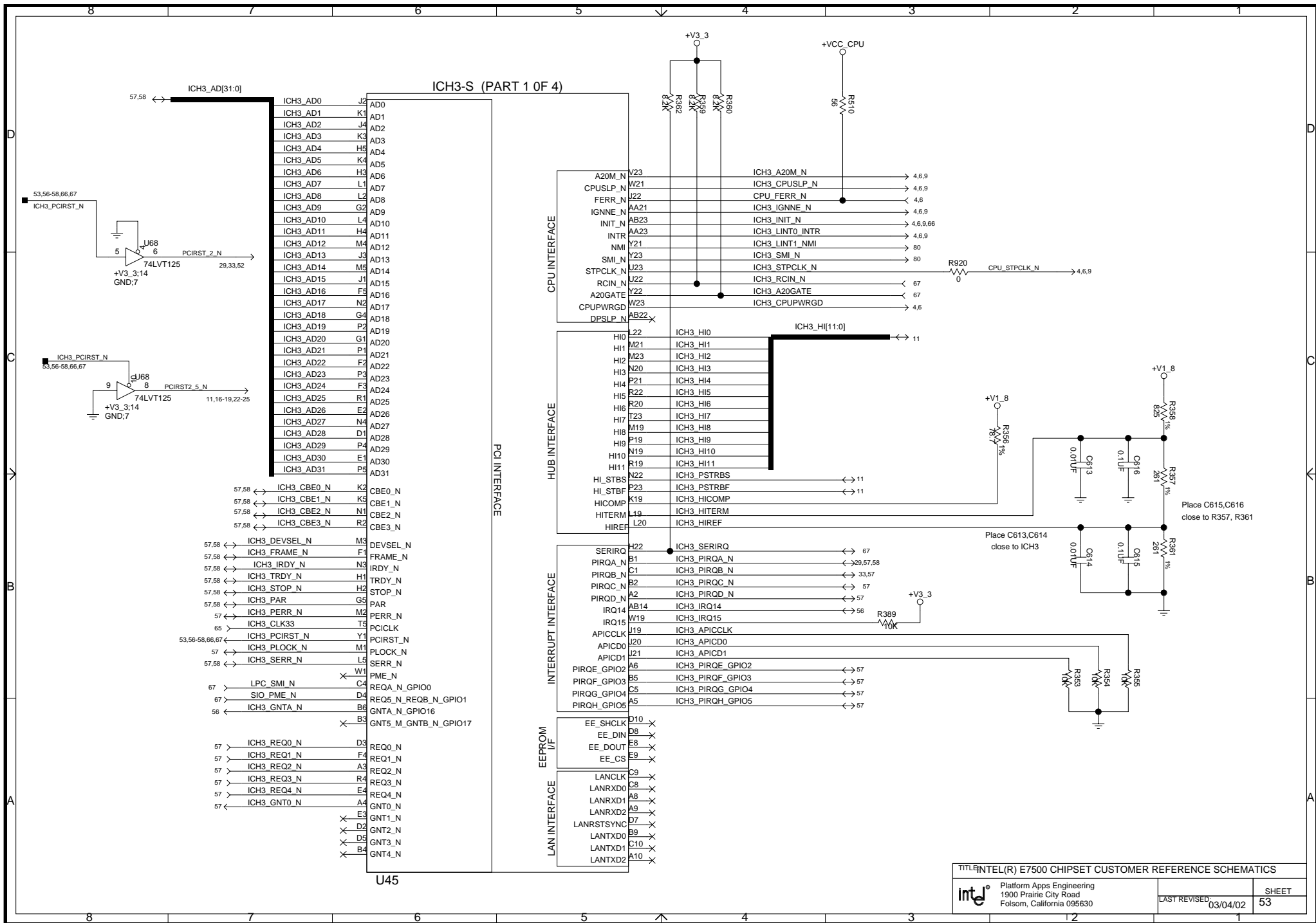
**Intel(R) E7500 CHIPSET CUSTOMER REFERENCE SCHEMATICS**

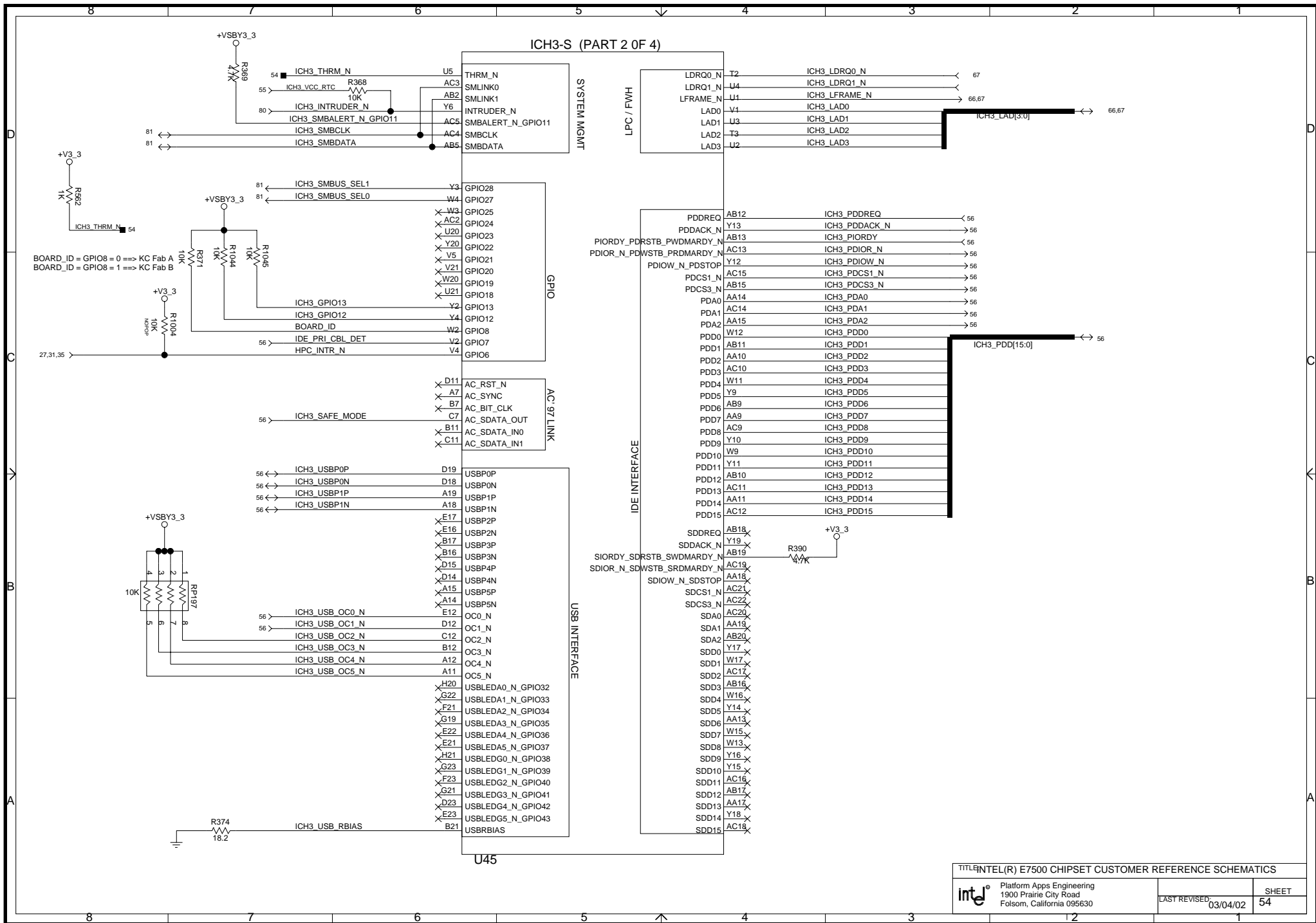
Platform Apps Engineering  
1900 Prairie City Road  
Folsom, California 95630

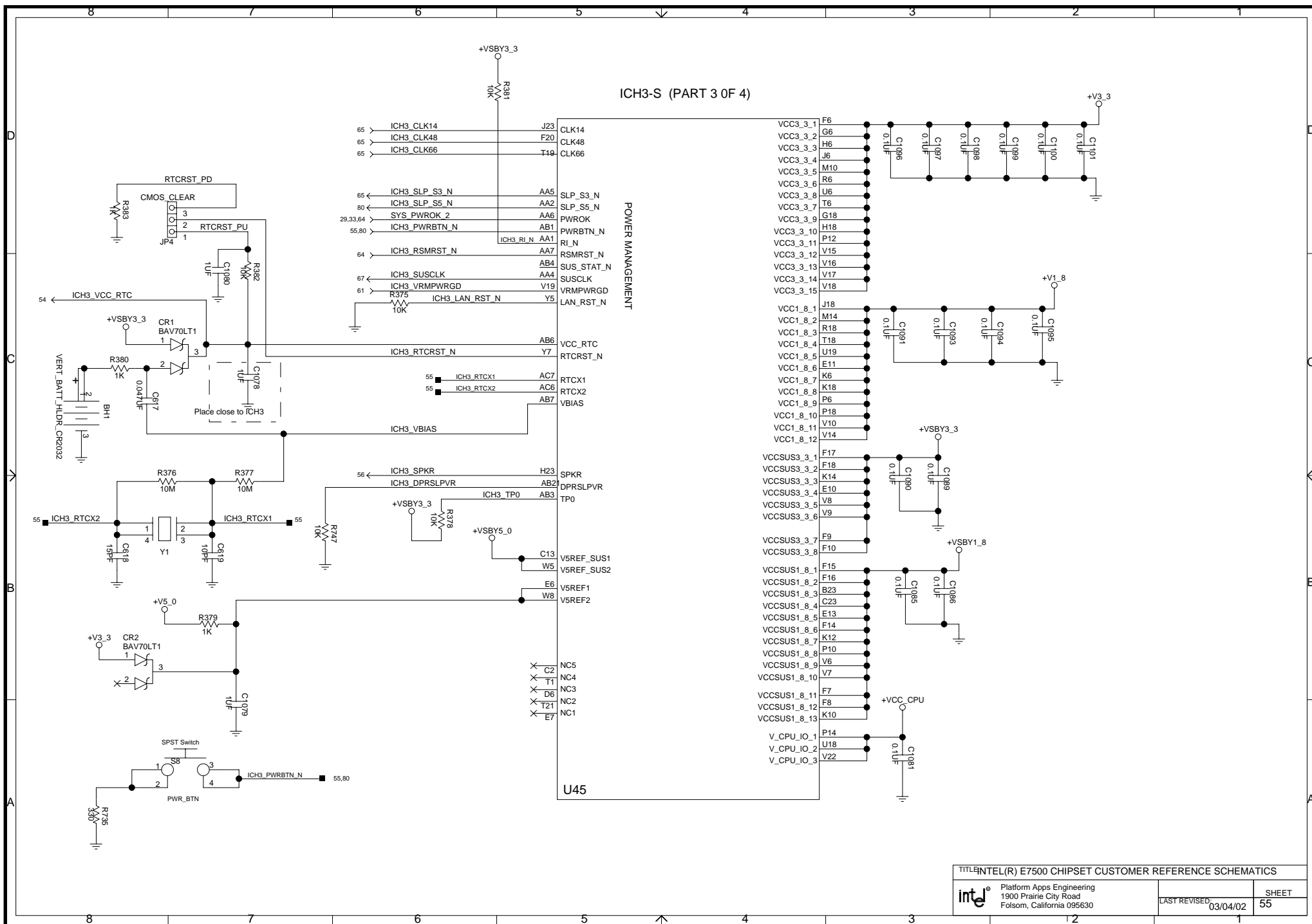
LAST REVISED: 03/04/02

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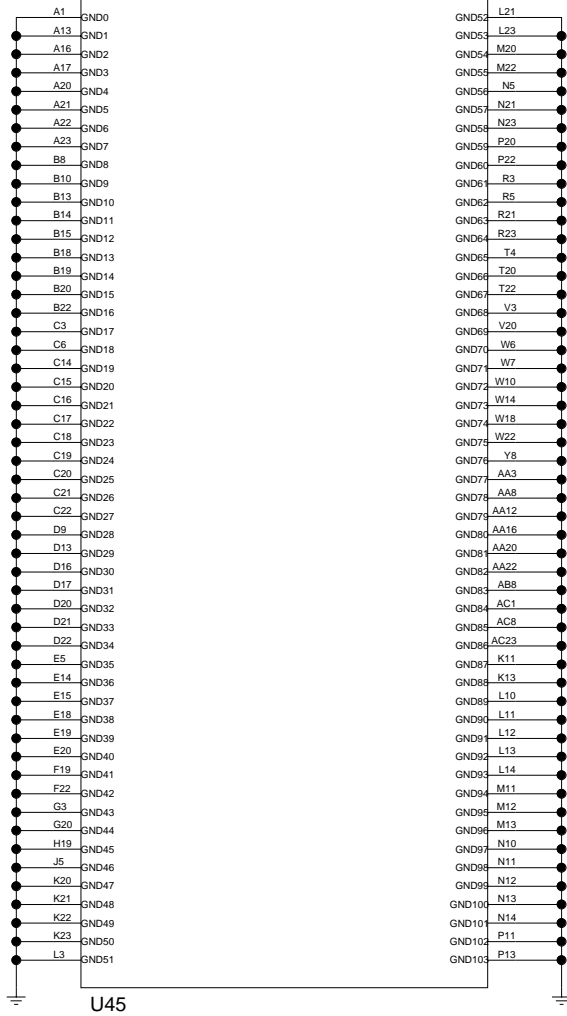




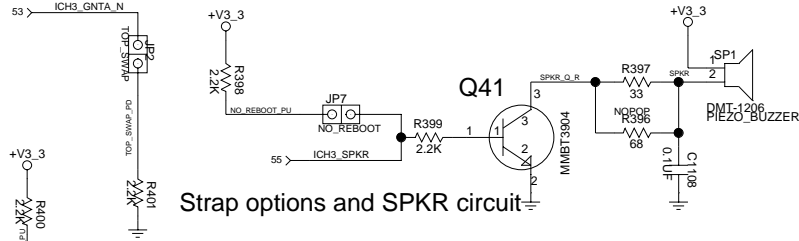




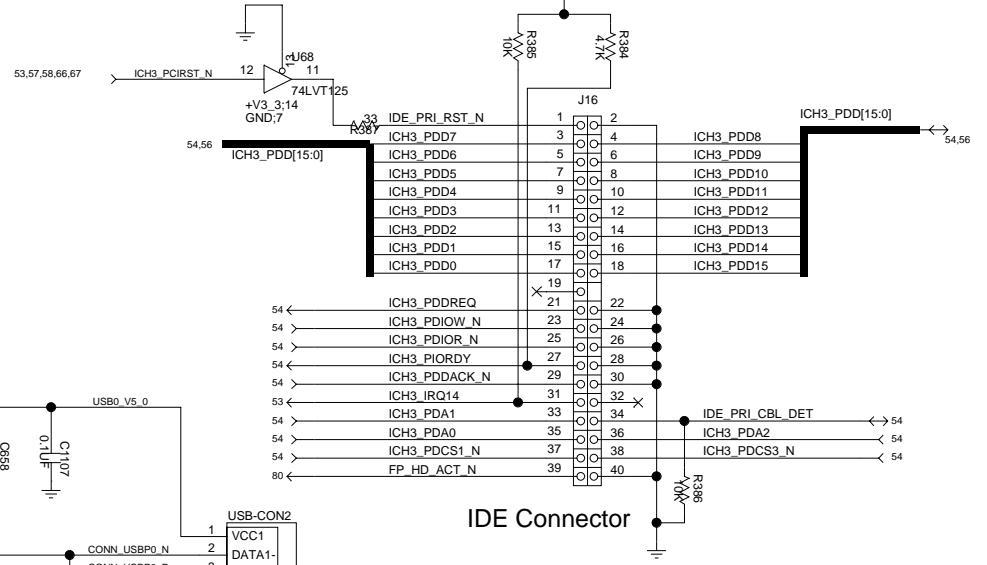
# ICH3-S (PART 4 OF 4)



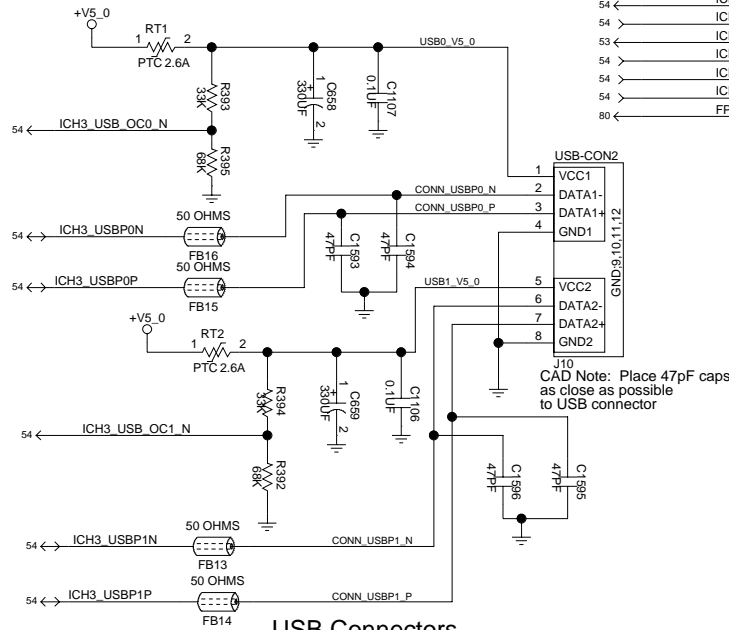
U45



Strap options and SPKR circuit

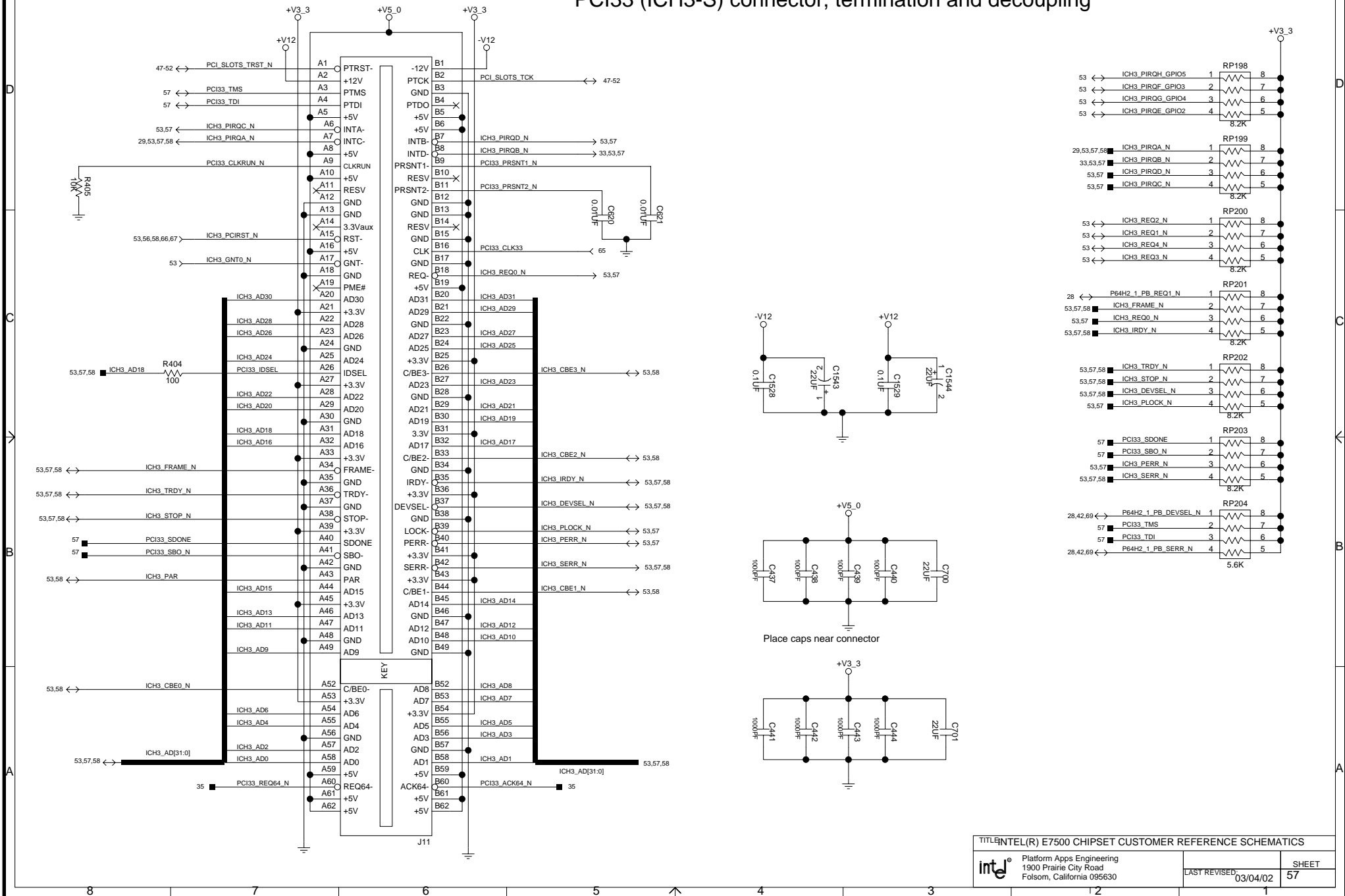


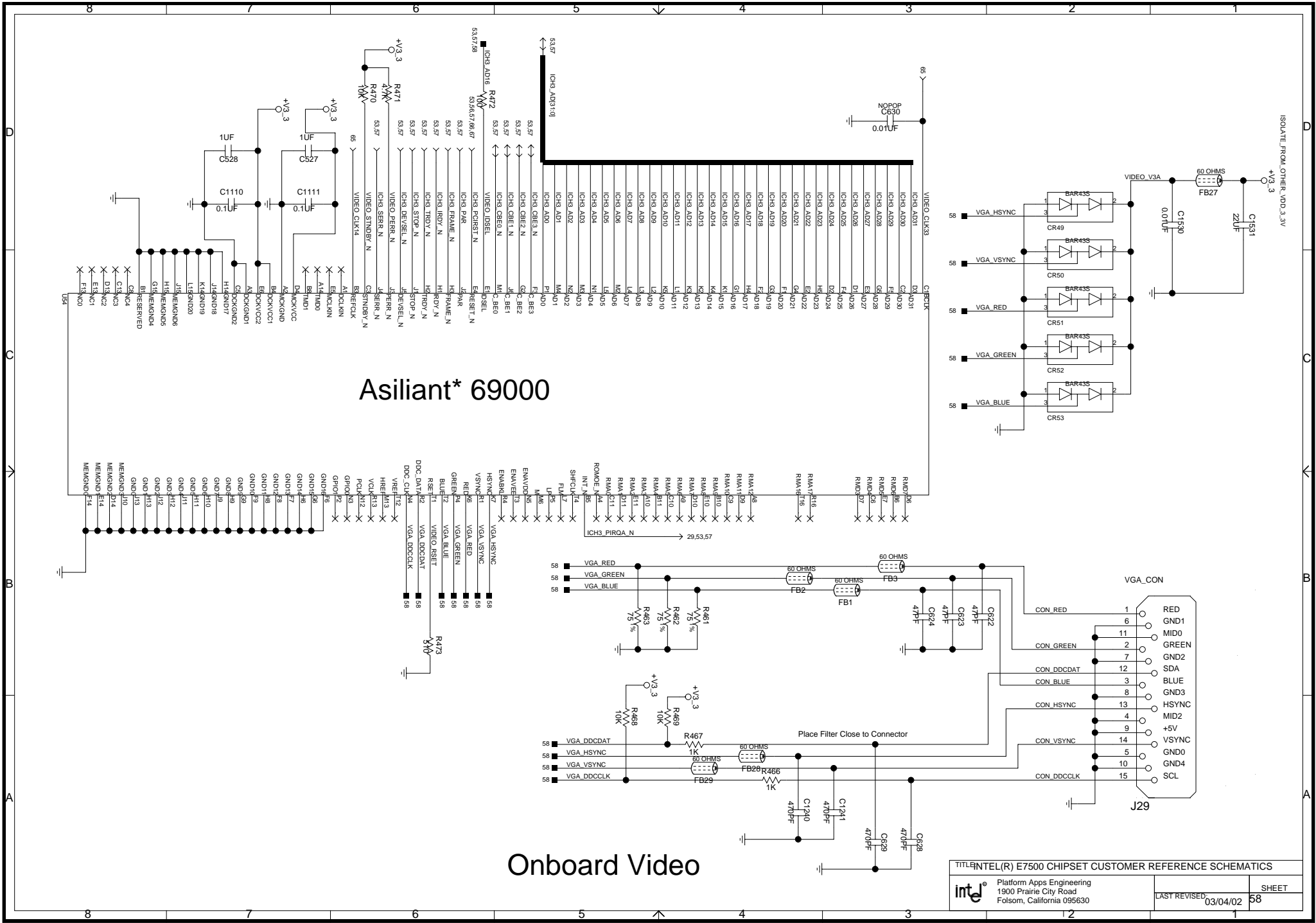
IDE Connector



USB Connectors

## PCI33 (ICH3-S) connector, termination and decoupling






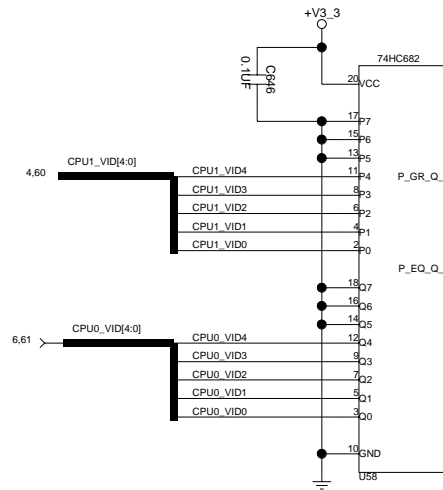
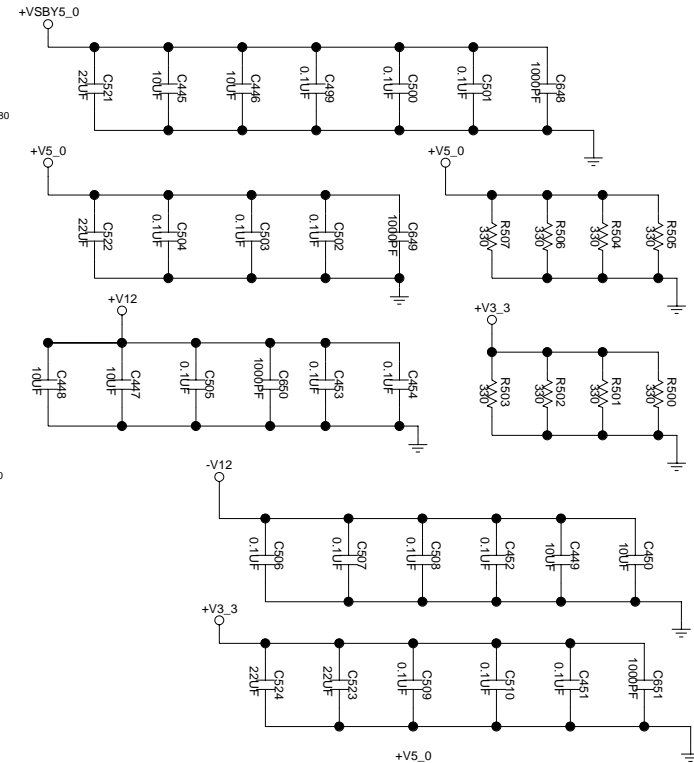
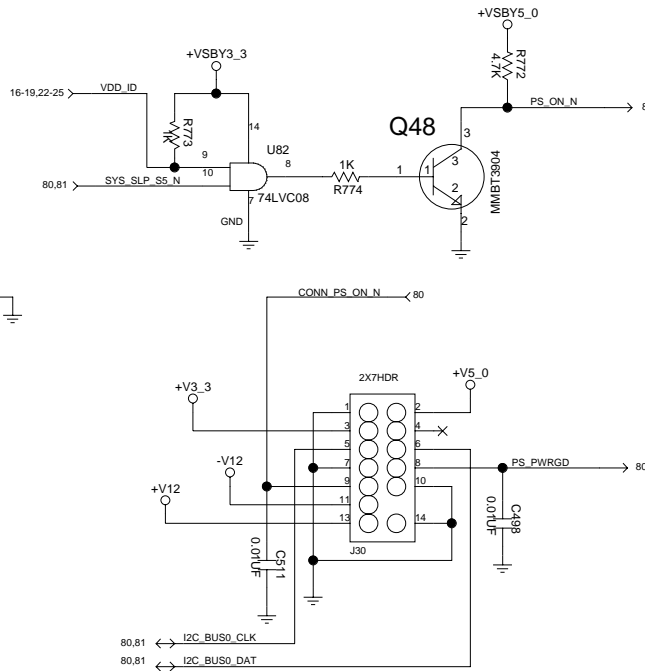
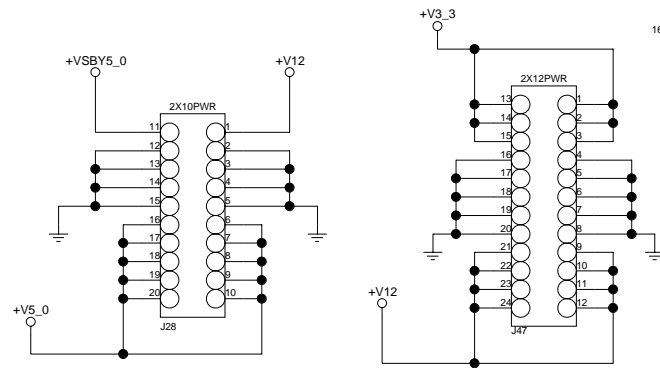
# Onboard Video



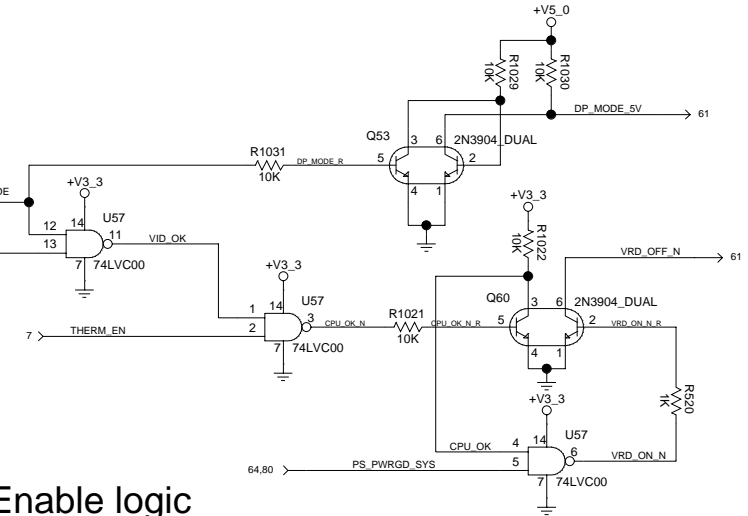
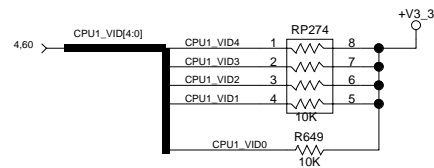


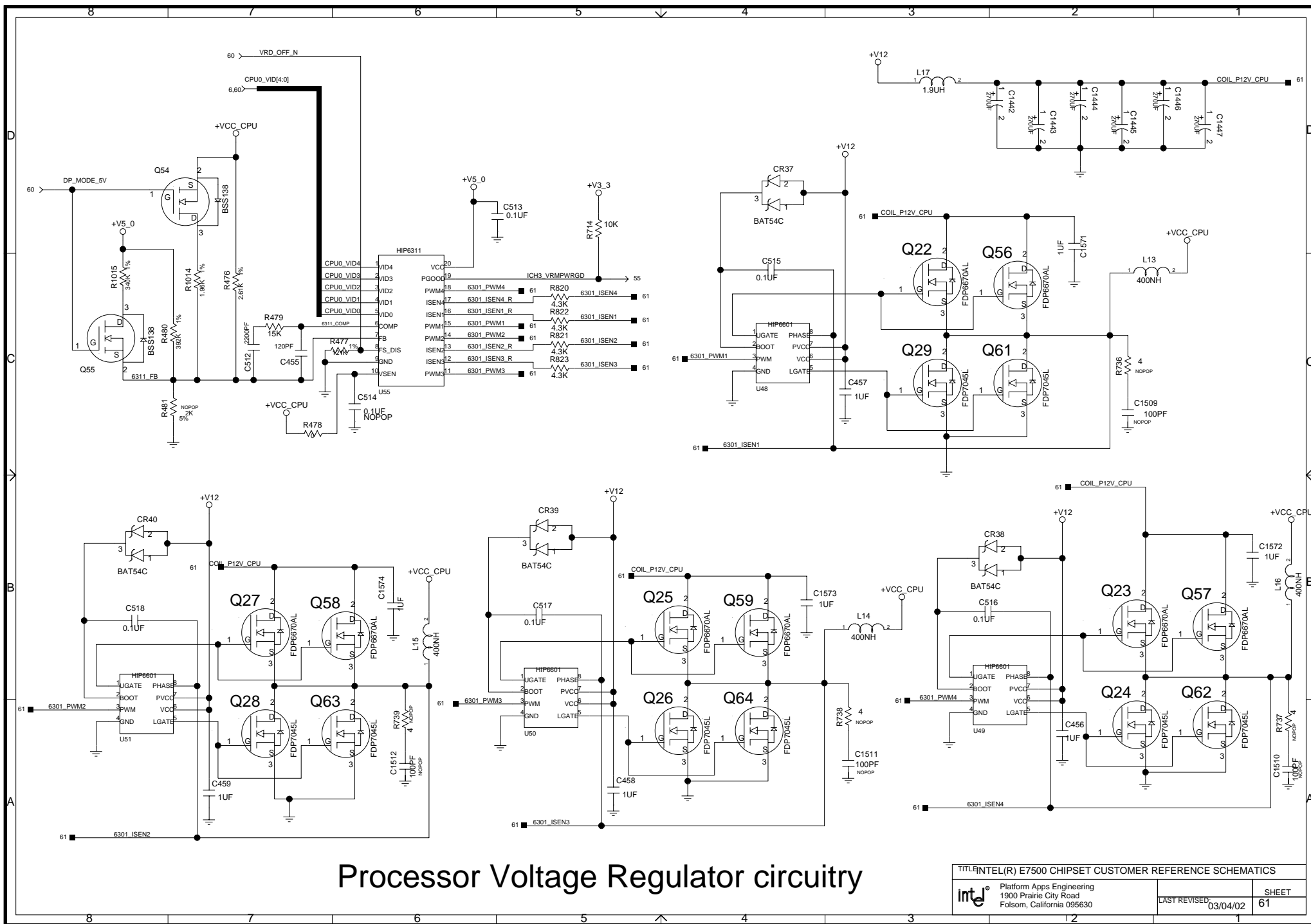
TITLE: INTEL(R) E7500 CHIPSET CUSTOMER REFERENCE SCHEMATICS		
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# Power Connectors

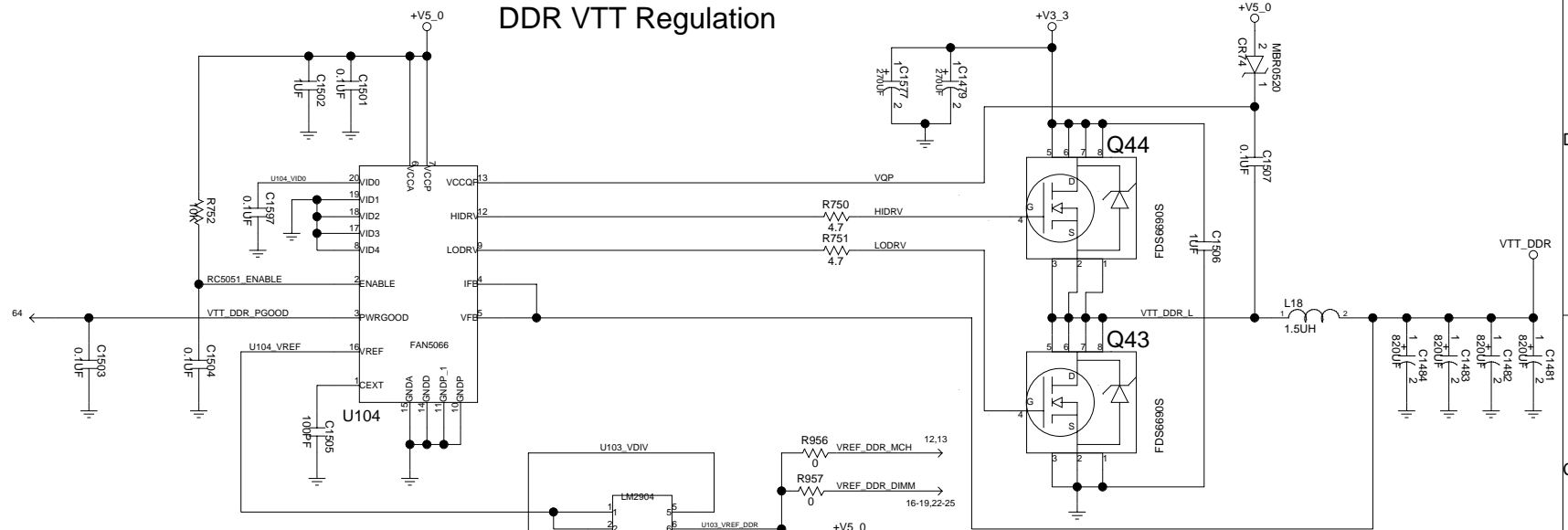


## VRD Enable logic





## DDR VTT Regulation



SCHOTTKY  
CR80

1929\_PG00D

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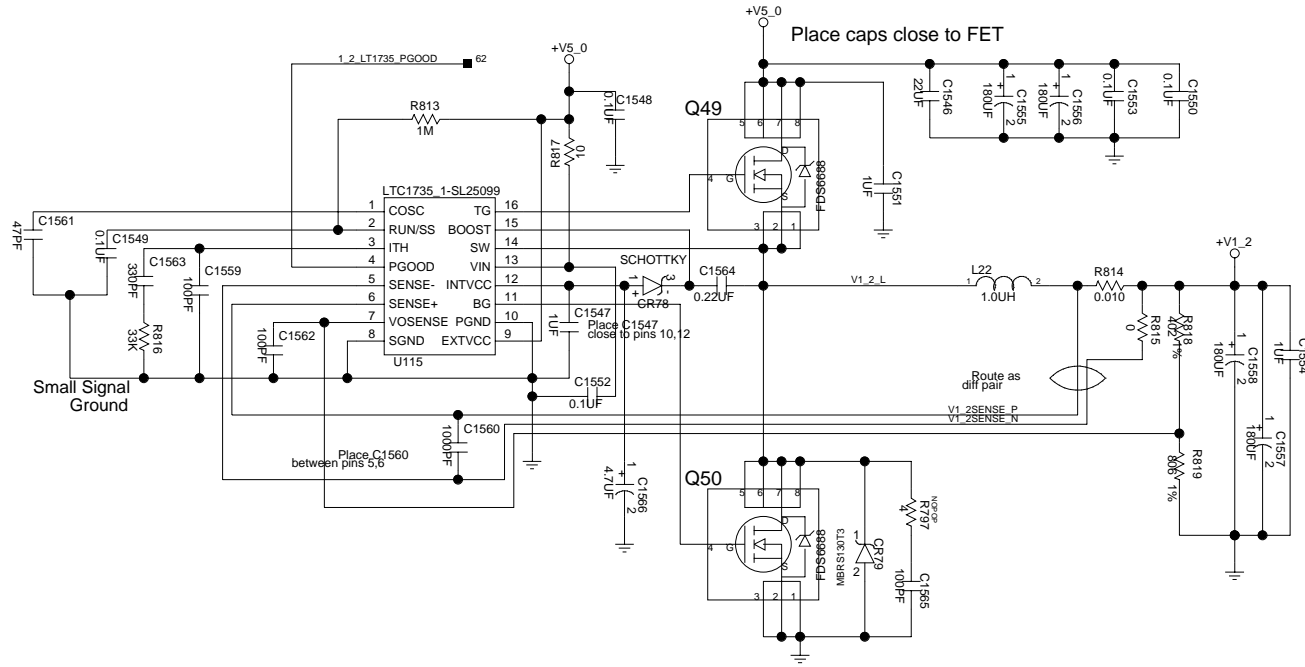
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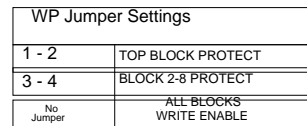
309

# V1.2 Regulation

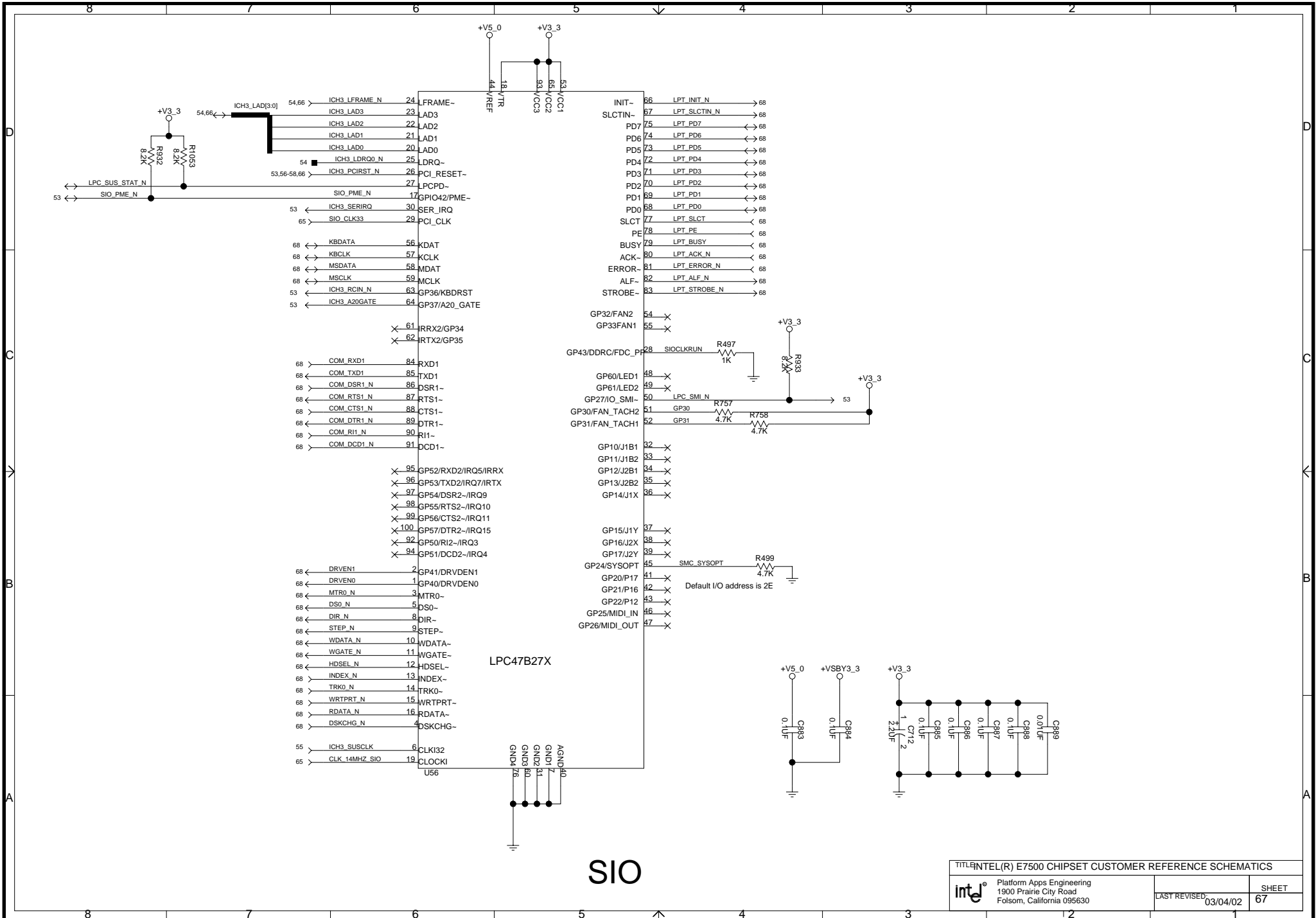












SIO

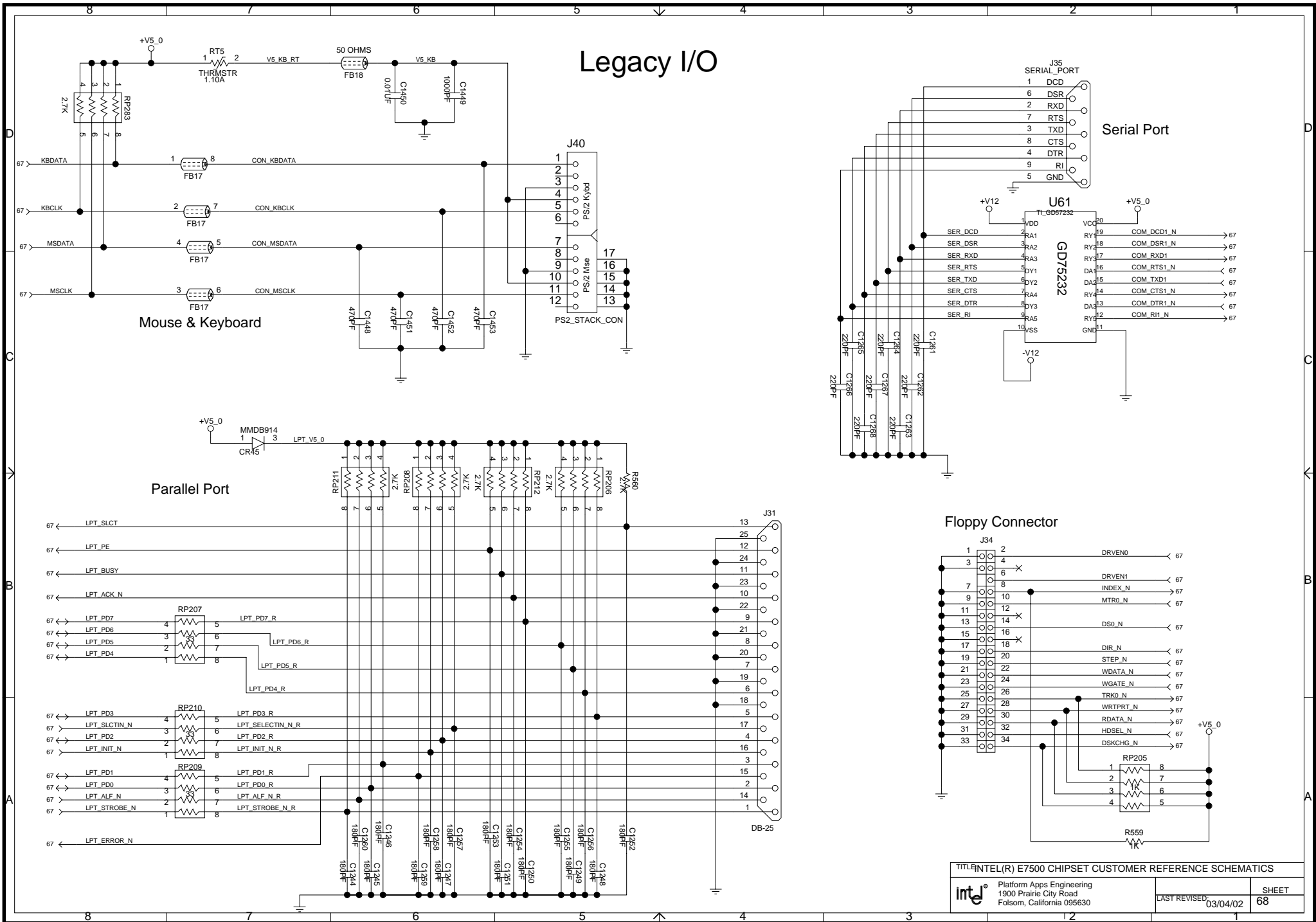
# Legacy I/O

## Mouse & Keyboard

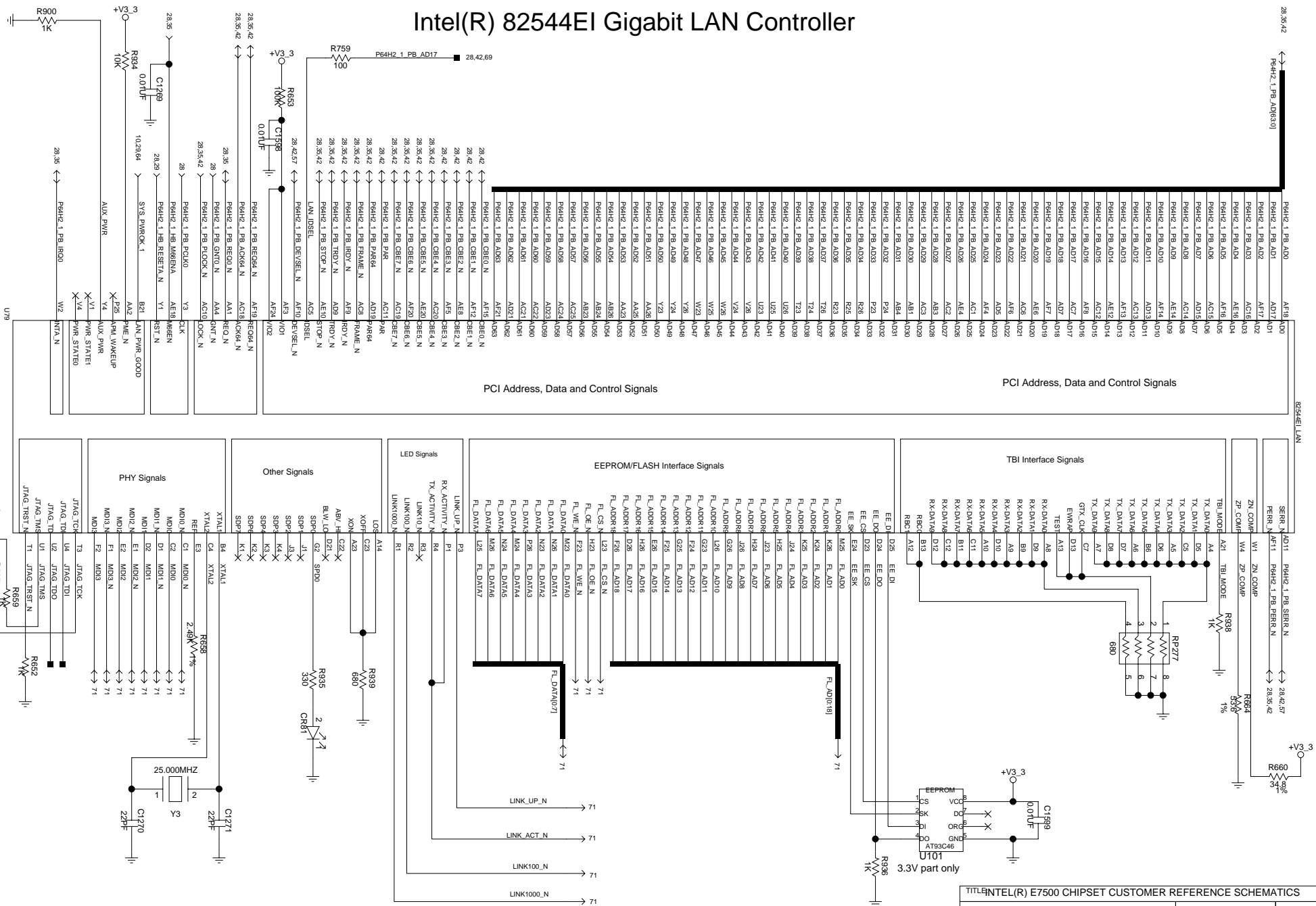
## Parallel Port

## Floppy Connector

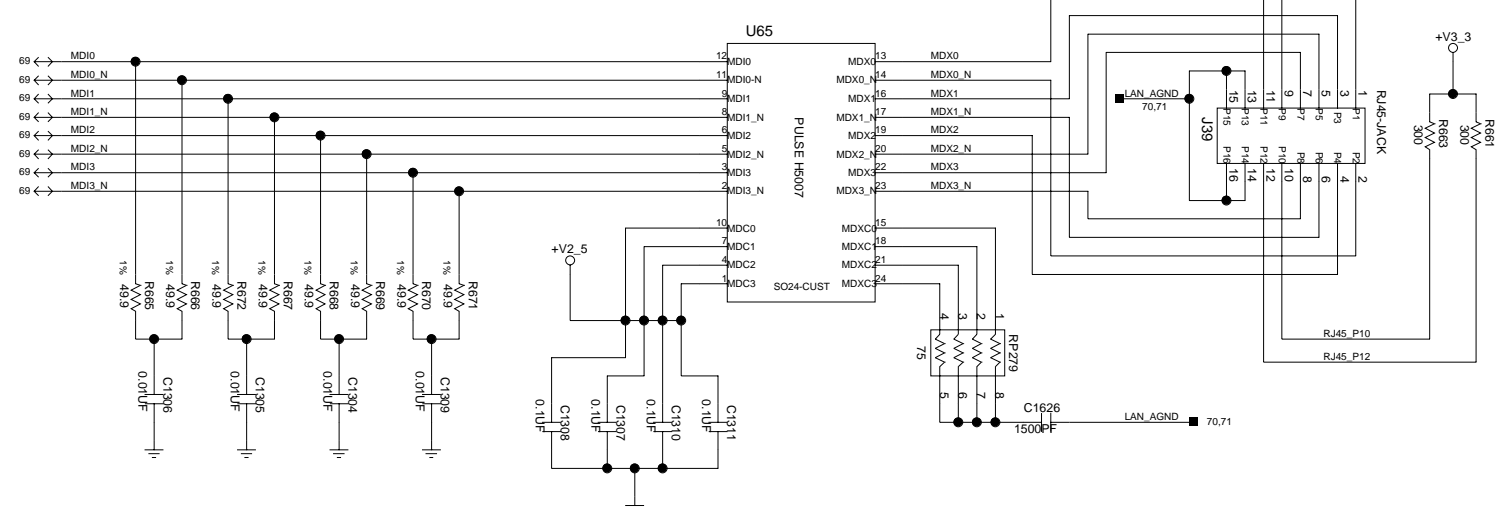
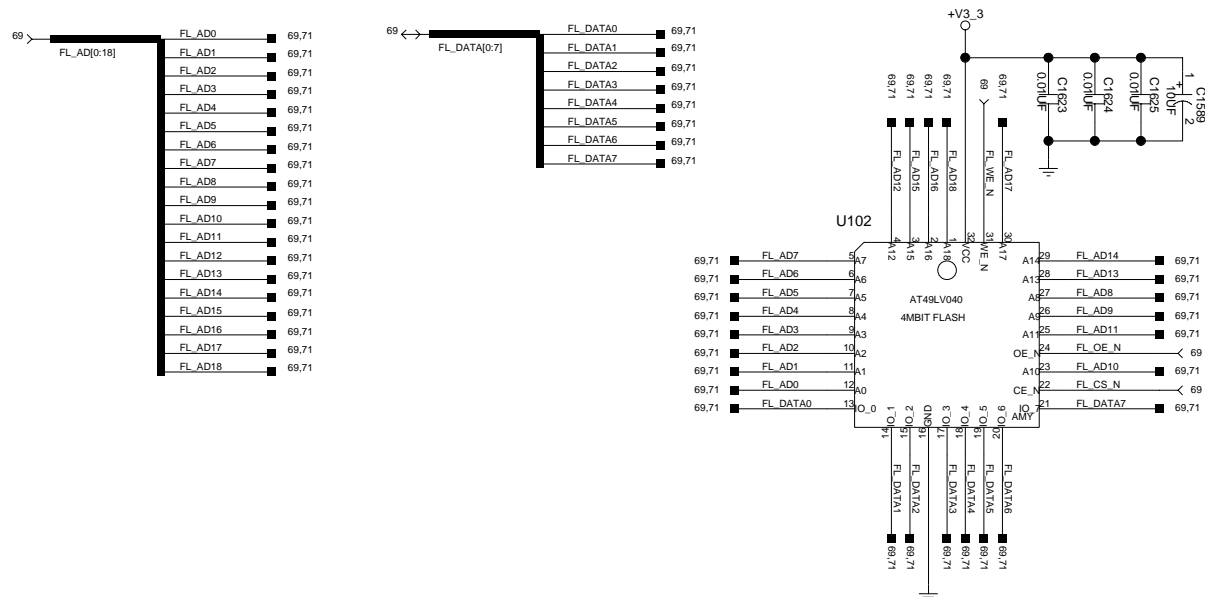
## Serial Port



## Intel(R) 82544EI Gigabit LAN Controller

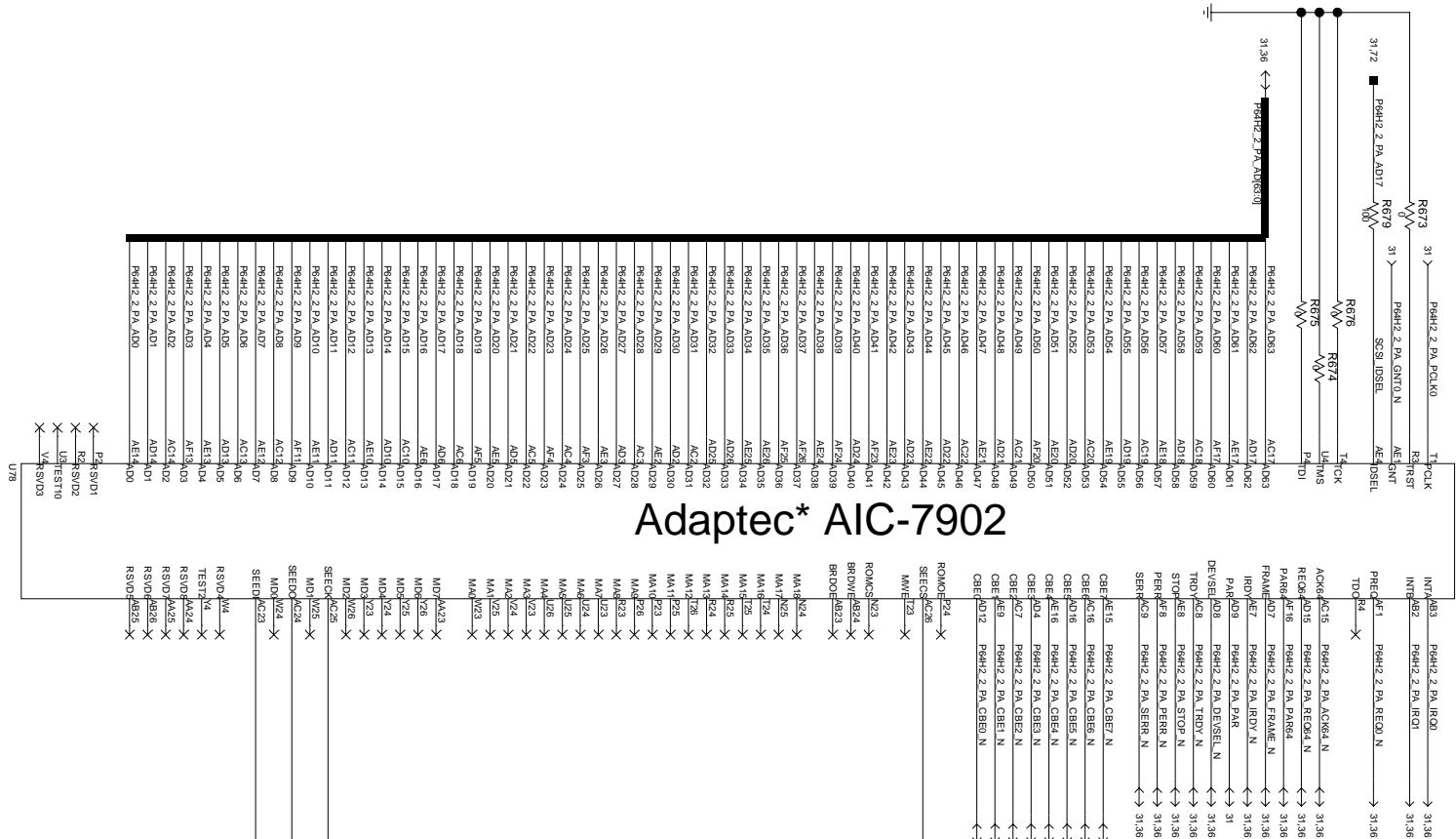


The schematic diagram shows the LAN and power supply sections of the circuit. The LAN section at the top features a 71-pin connector labeled "LAN AGND" connected to a series of capacitors: C1R05 (1000pF), C1R04 (1000pF), C1R03 (1000pF), C1R02 (1000pF), C1R01 (100pF), C1R00 (4.7nF), C1R06 (100pF), C1R07 (100pF), and C1R08 (100pF). These capacitors are connected to a common ground line. A 70-pin connector labeled "FB30" is also shown, connected to a common ground line. The power supply section at the bottom shows two input pins: "+V3.3" and "+V1.5". The "+V3.3" pin is connected to a 22uF capacitor (C1587) to ground. The "+V1.5" pin is connected to a 22uF capacitor (C1588) to ground. The output of the "+V3.3" capacitor is connected to the "IN" pin of the LT1587CM1.5 regulator. The "OUT" pin of the regulator is connected to the "+V1.5" pin. The "GND" pin of the regulator is connected to ground. The "U119" label is also present near the ground connection.

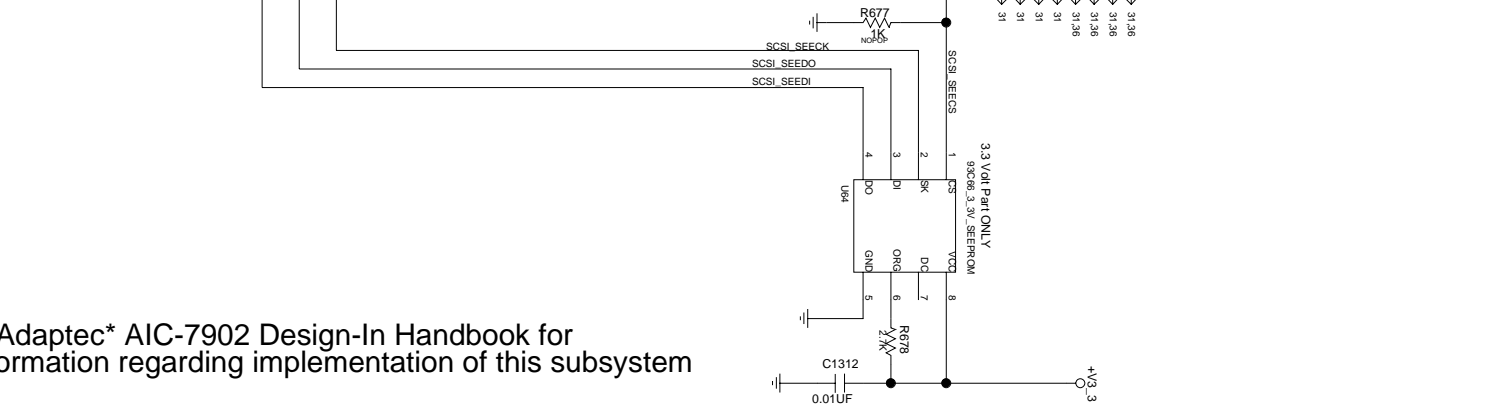


# LAN EEPROM, Magnetics and Connector

# PCI and Memory I/F



Adaptec\* AIC-7902



SCSI Controller

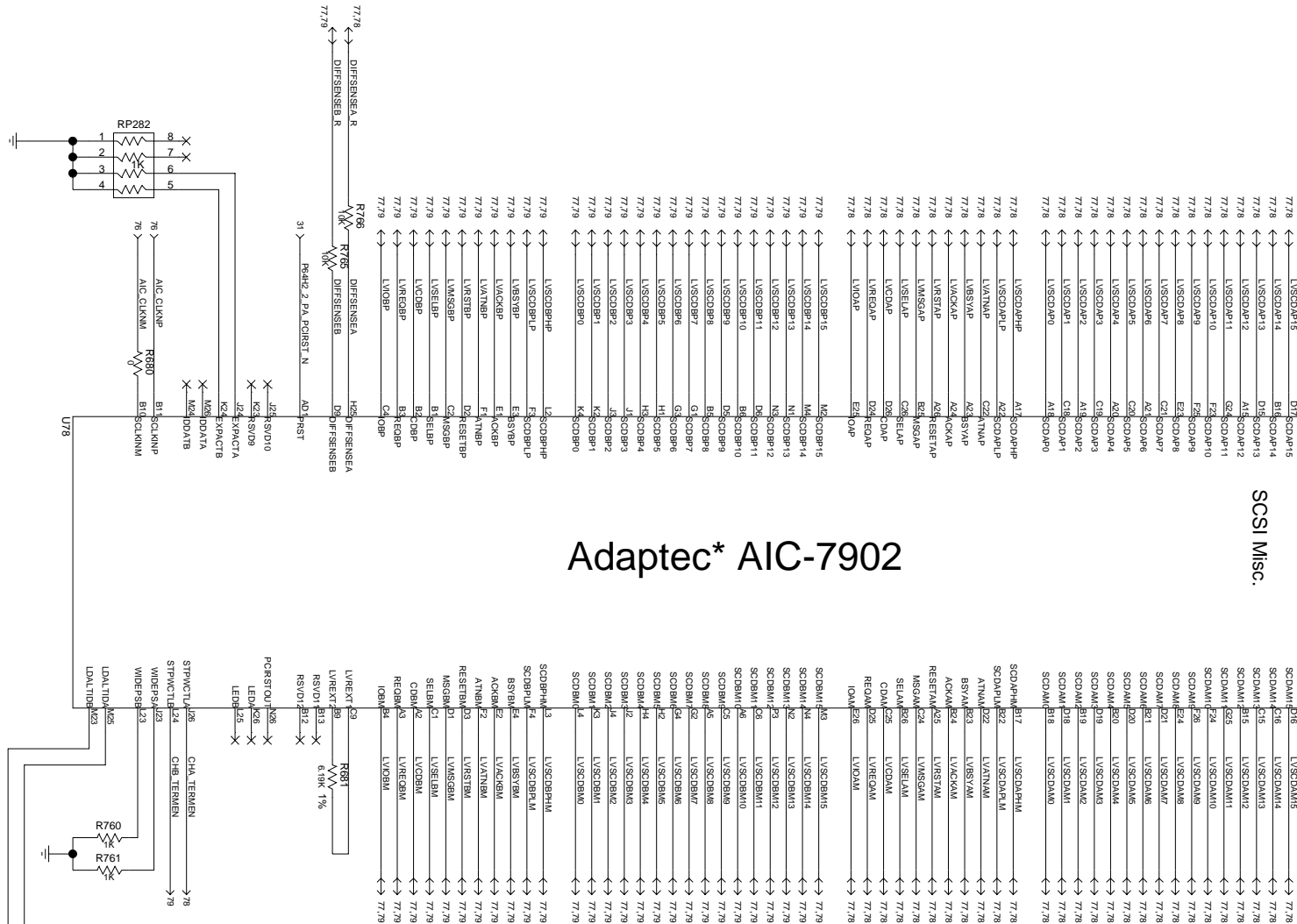
See Adaptec\* AIC-7902 Design-In Handbook for up-to-date information regarding implementation of this subsystem

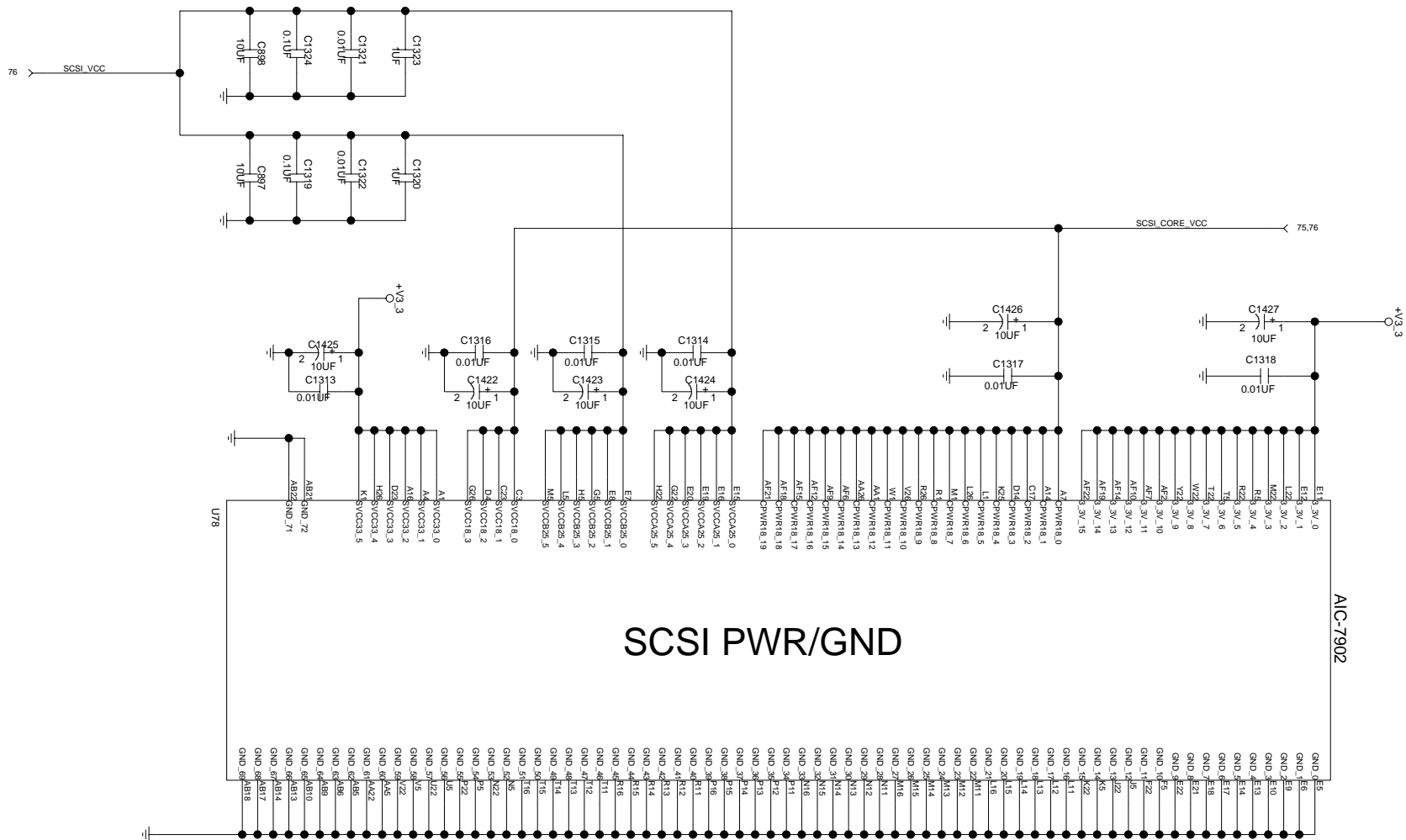
# SCSI Misc.

## Adaptec\* AIC-7902

### SCSI Controller

See Adaptec\* AIC-7902 Design-In Handbook for up-to-date information regarding implementation of this subsystem






## SCSI PWR/GND

AIC-7902

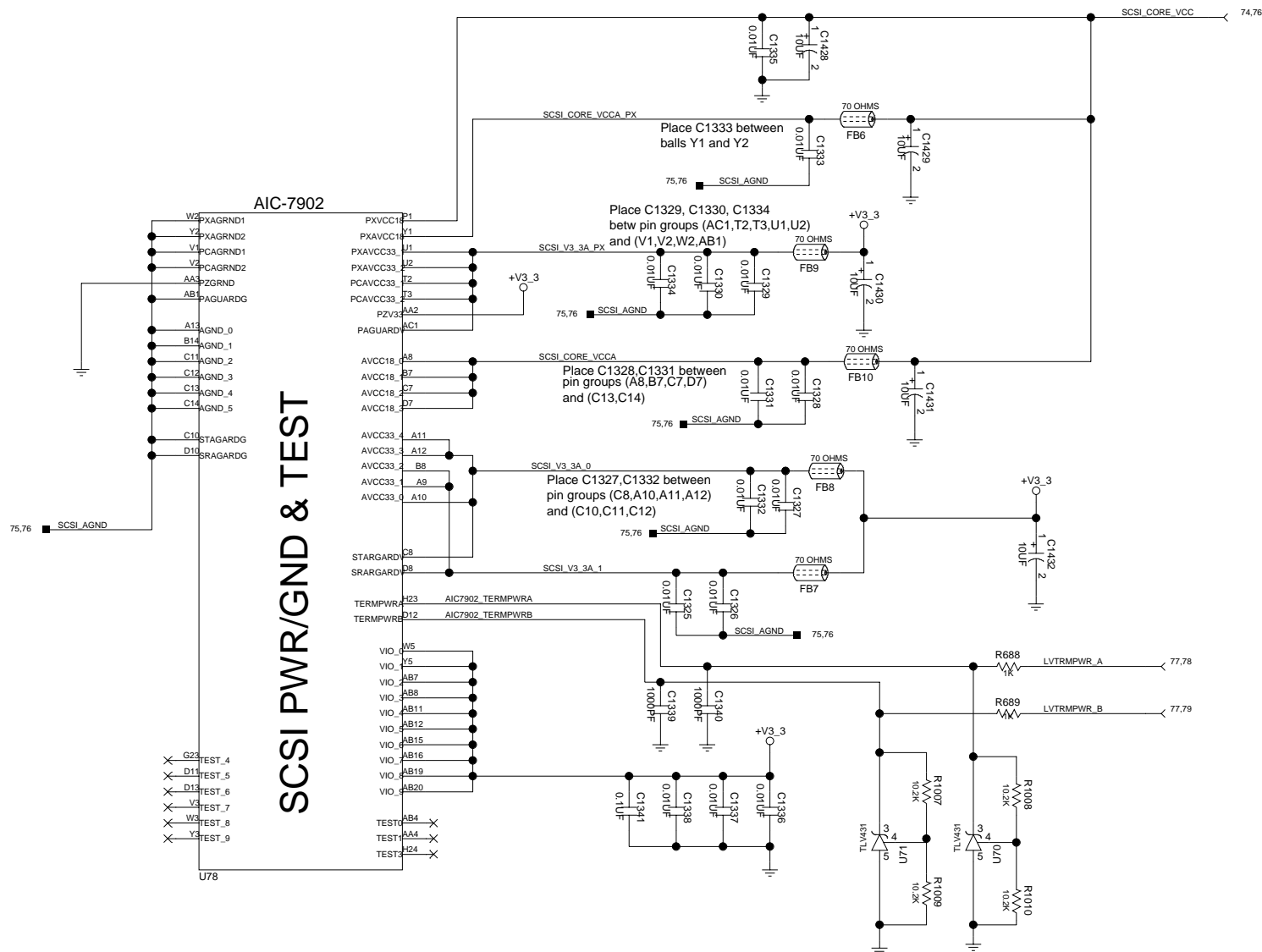
See Adaptec\* AIC-7902 Design-In Handbook for  
up-to-date information regarding implementation of this subsystem

## SCSI Controller

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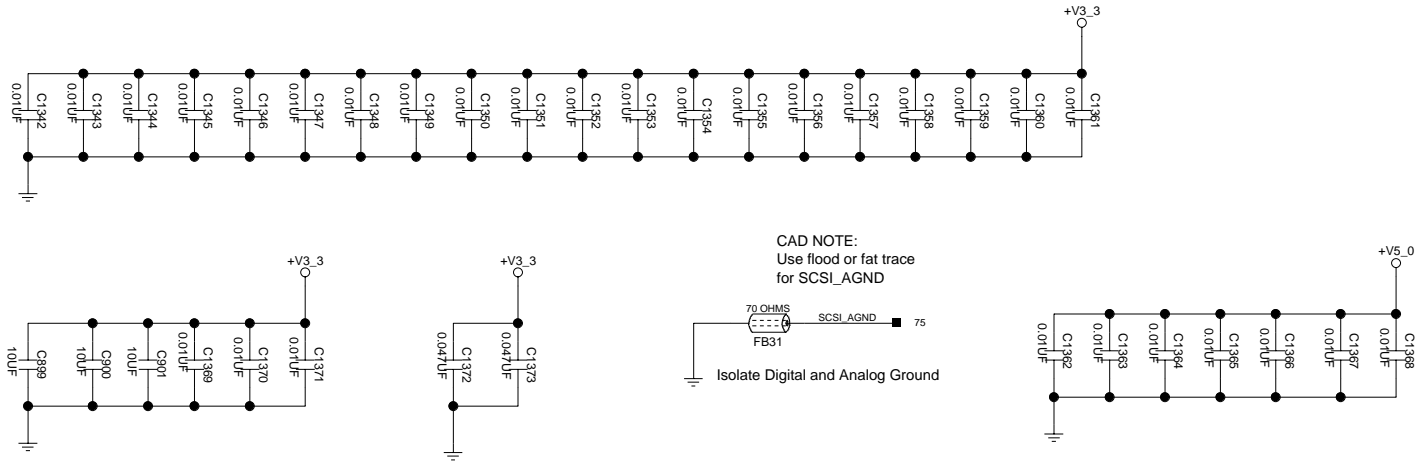


CAD NOTE:  
Use flood or fat trace  
for AGND

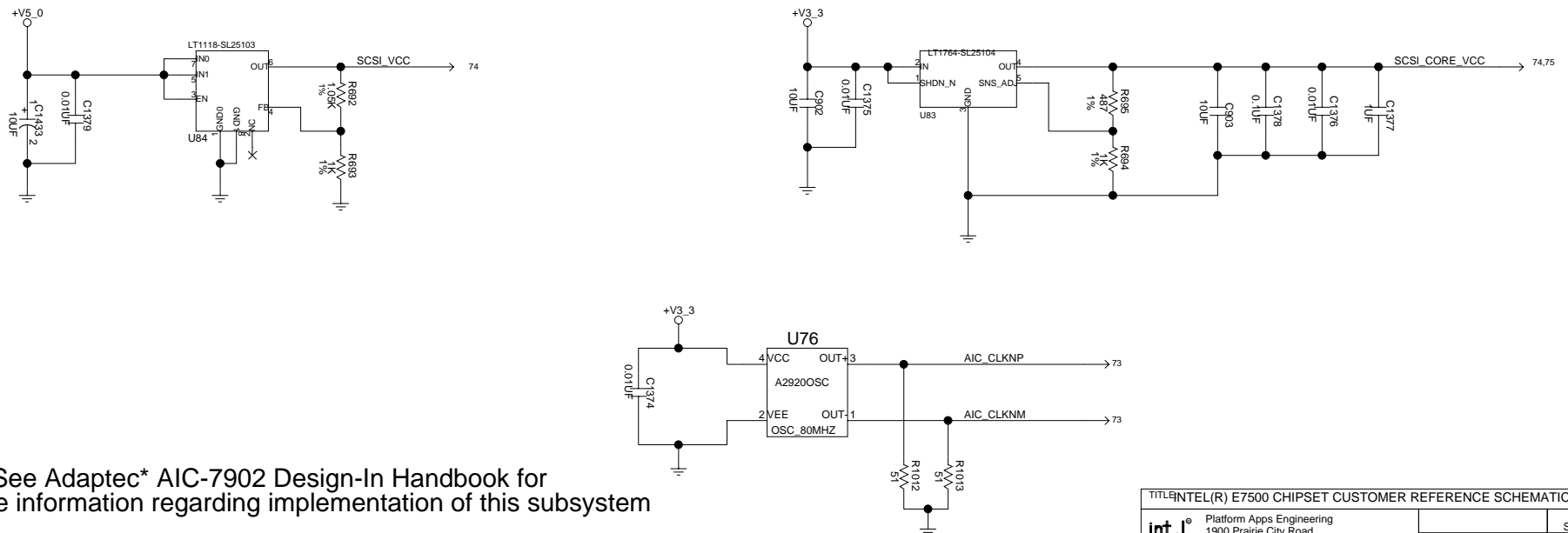


## SCSI Controller

## AIC-7902 SCSI Decoupling

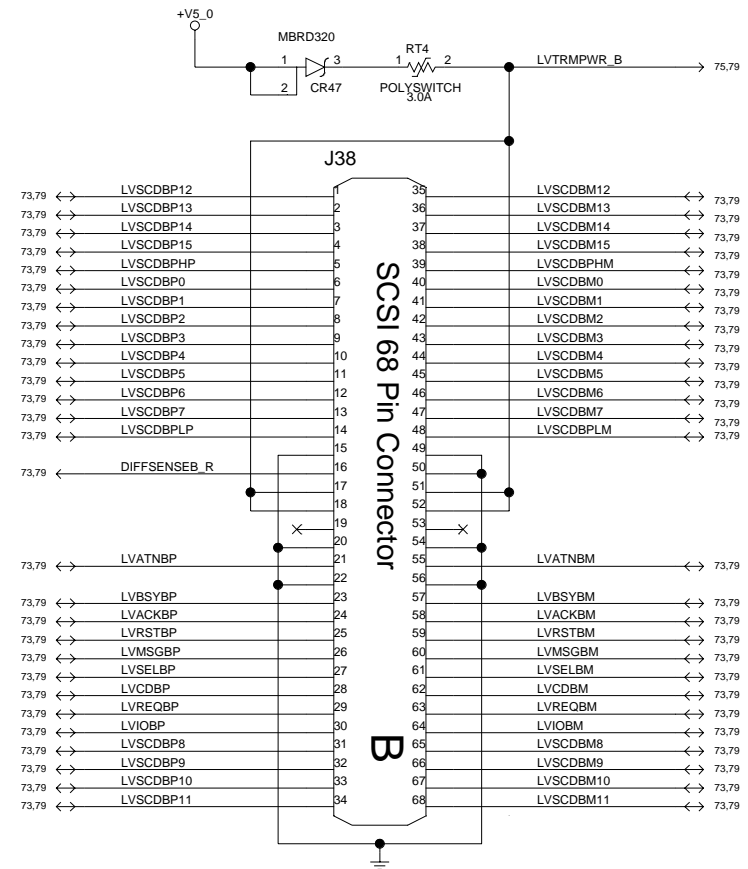
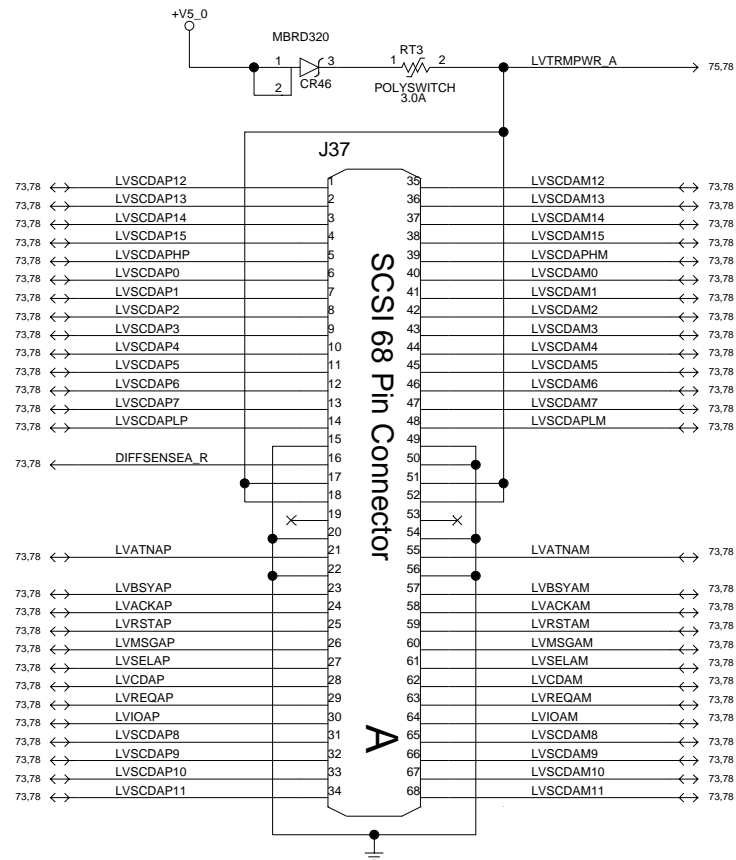


## Voltage Regulators and SCSI Clock



See Adaptec\* AIC-7902 Design-In Handbook for up-to-date information regarding implementation of this subsystem


# SCSI Connectors A and B



See Adaptec\* AIC-7902 Design-In Handbook for up-to-date information regarding implementation of this subsystem

## A



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**LVD/SE Termination for SCSI Channel B**

The schematic shows three DS2119M transceivers (U96, U97, U98) connected to a SCSI bus. The transceivers are configured for LVD/SE termination. The signal traces are as follows:

- U96:** LVMSGBP (2), LVSCDBP9 (9), LVSCDBP11 (11), LVSCDBP10 (18), LVSCDBP8 (20), LVREOBP (23), LVSELBP (25).
- U97:** LVSCDBP4 (2), LVSCDBP6 (4), LVSCDBLP (7), LVACKBP (9), LVIRSTBP (11), LVBSYBP (18), LVATNBP (20), LVSCDBP7 (23), LVSCDBP5 (25).
- U98:** LVSCDBP12 (2), LVSCDBP14 (4), LVSCDBP13 (7), LVSCDBP1 (9), LVSCDBP3 (11), LVSCDBP2 (18), LVSCDBP0 (20), LVSCDBP15 (23), LVSCDBP13 (25).

The diagram also includes termination resistors (R1-R9) and capacitors (C1387, C1388, C1389, C1390, C1395) connected to the signal lines. Power and ground connections for the transceivers are also shown.

See Adaptec\* AIC-7902 Design-In Handbook for up-to-date information regarding implementation of this subsystem

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**LVD/SE Termination for SCSI Channel B**

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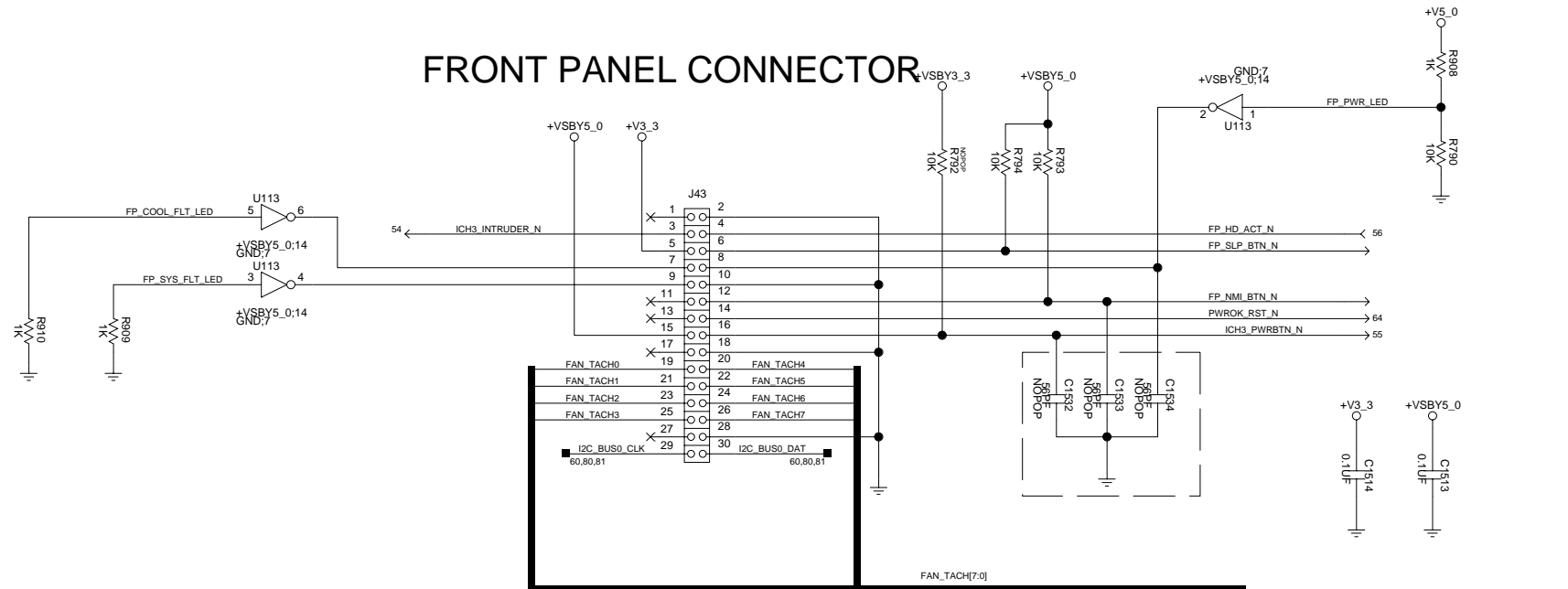
**INTel(R) E7500 CHIPSET CUSTOMER REFERENCE SCHEMATICS**

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Folsom, California 95630

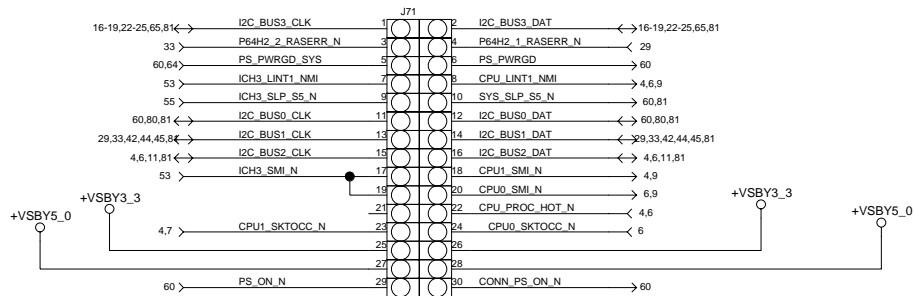
LAST REVISED: 03/04/02

SHEET 79

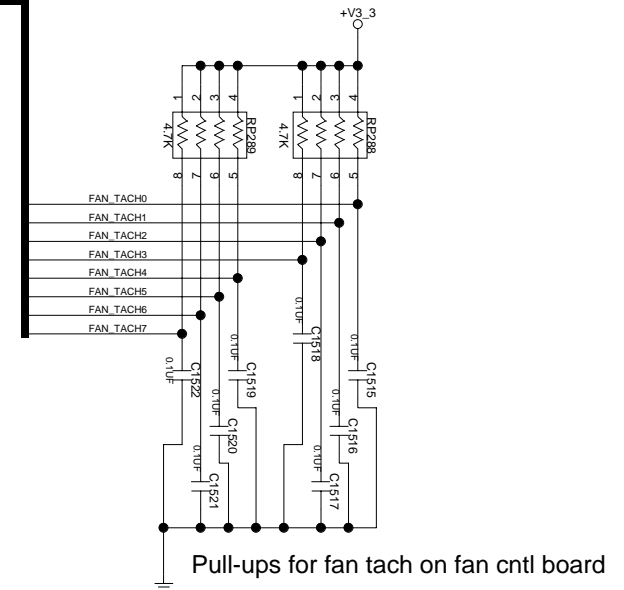
# FRONT PANEL CONNECTOR



Install jumpers to short pin pairs  
5 and 6, 7 and 8, 9 and 10, 17 and 18,  
19 and 20, 29 and 30

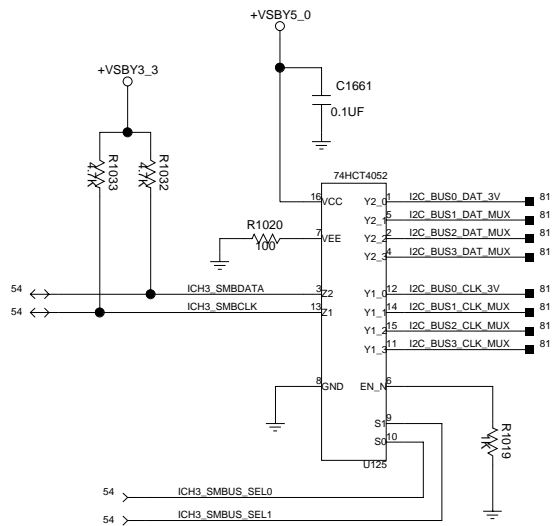


For Test Purposes Only



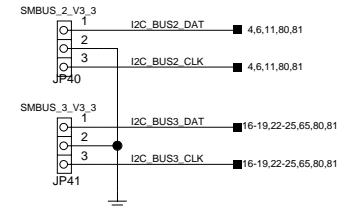
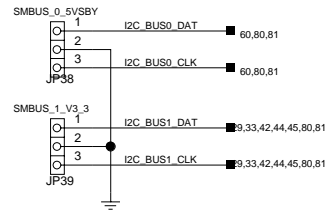
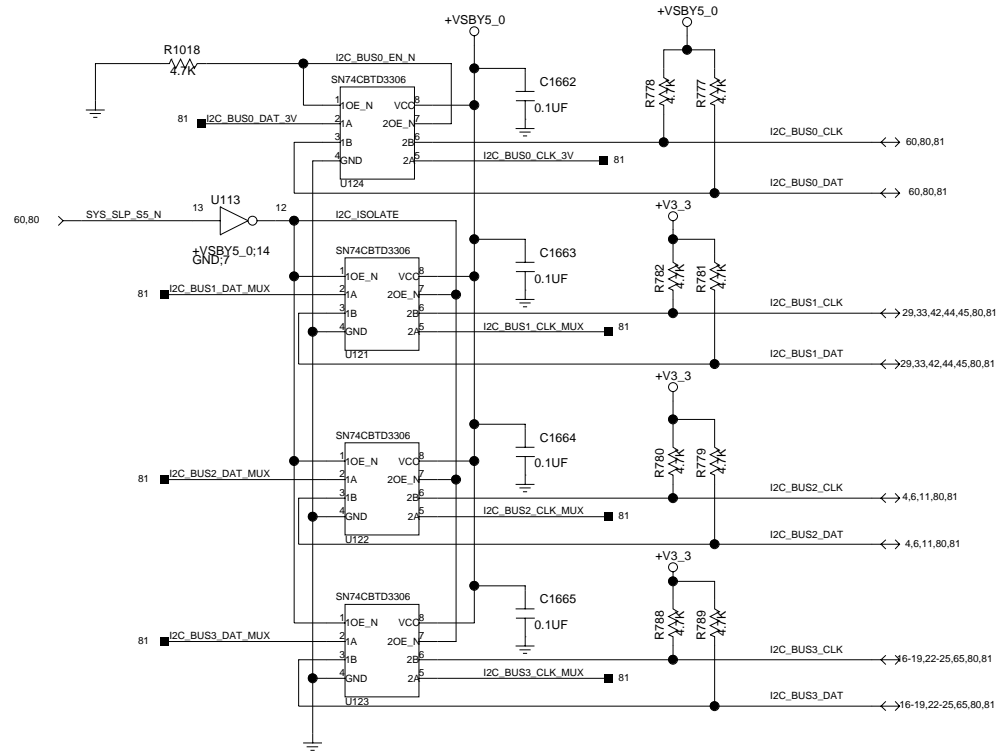
Pull-ups for fan tach on fan cntl board

## SMBus Mux

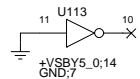
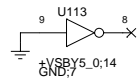
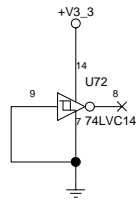


SEL1	SEL0	SMBus Partition
0	0	Bus 0
0	1	Bus 1
1	0	Bus 2
1	1	Bus 3 (default)

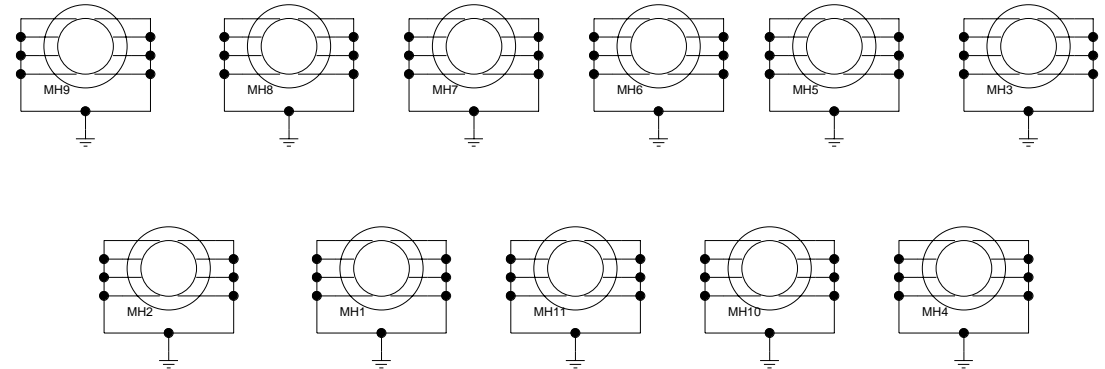
## SMBus Isolation and Voltage Translation



## SPARE GATES



## Mounting Holes



## Fiducial marks

